

Fig 1

Transmit 201 Total Receive 202

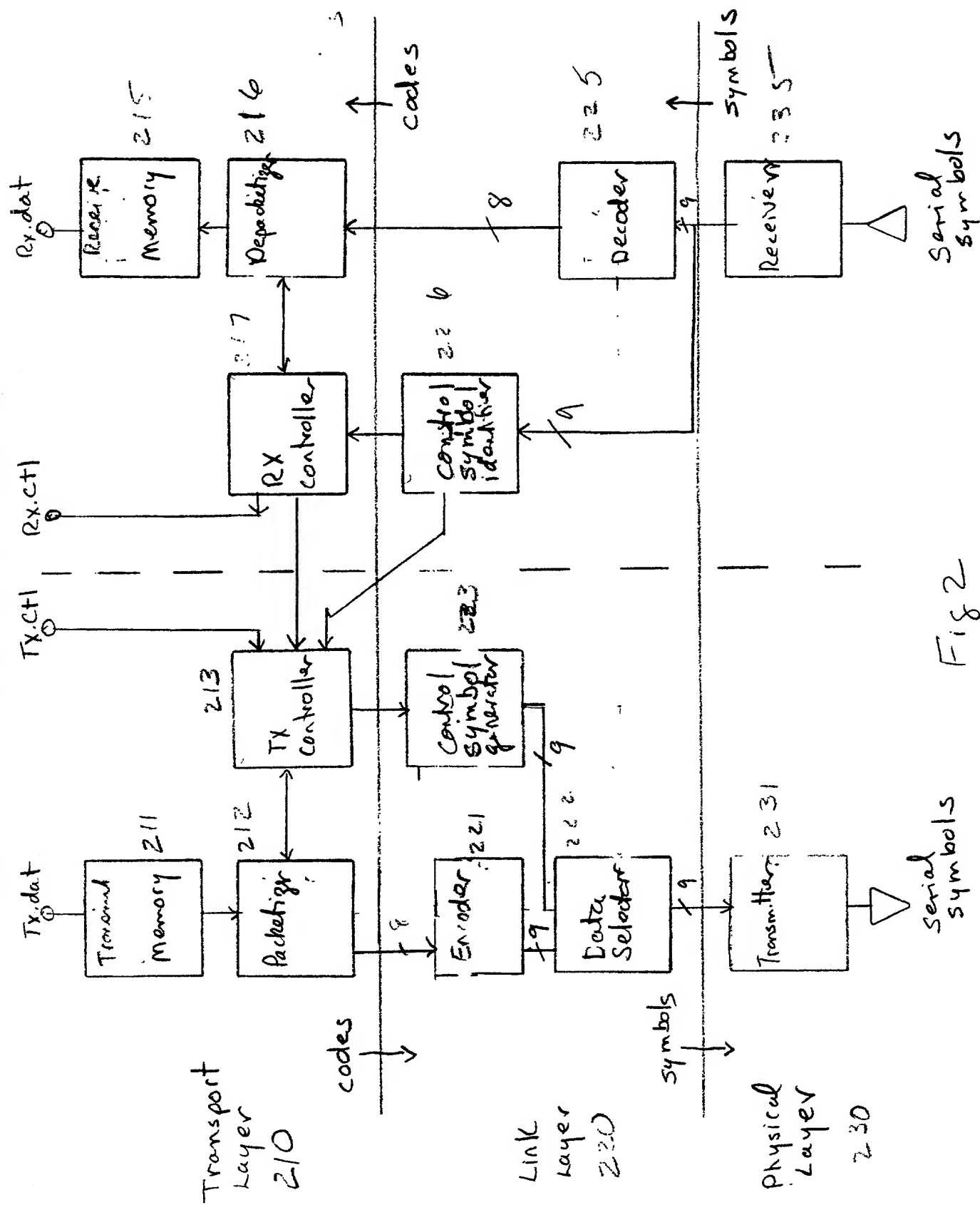


Fig 2

Physical Layer 230

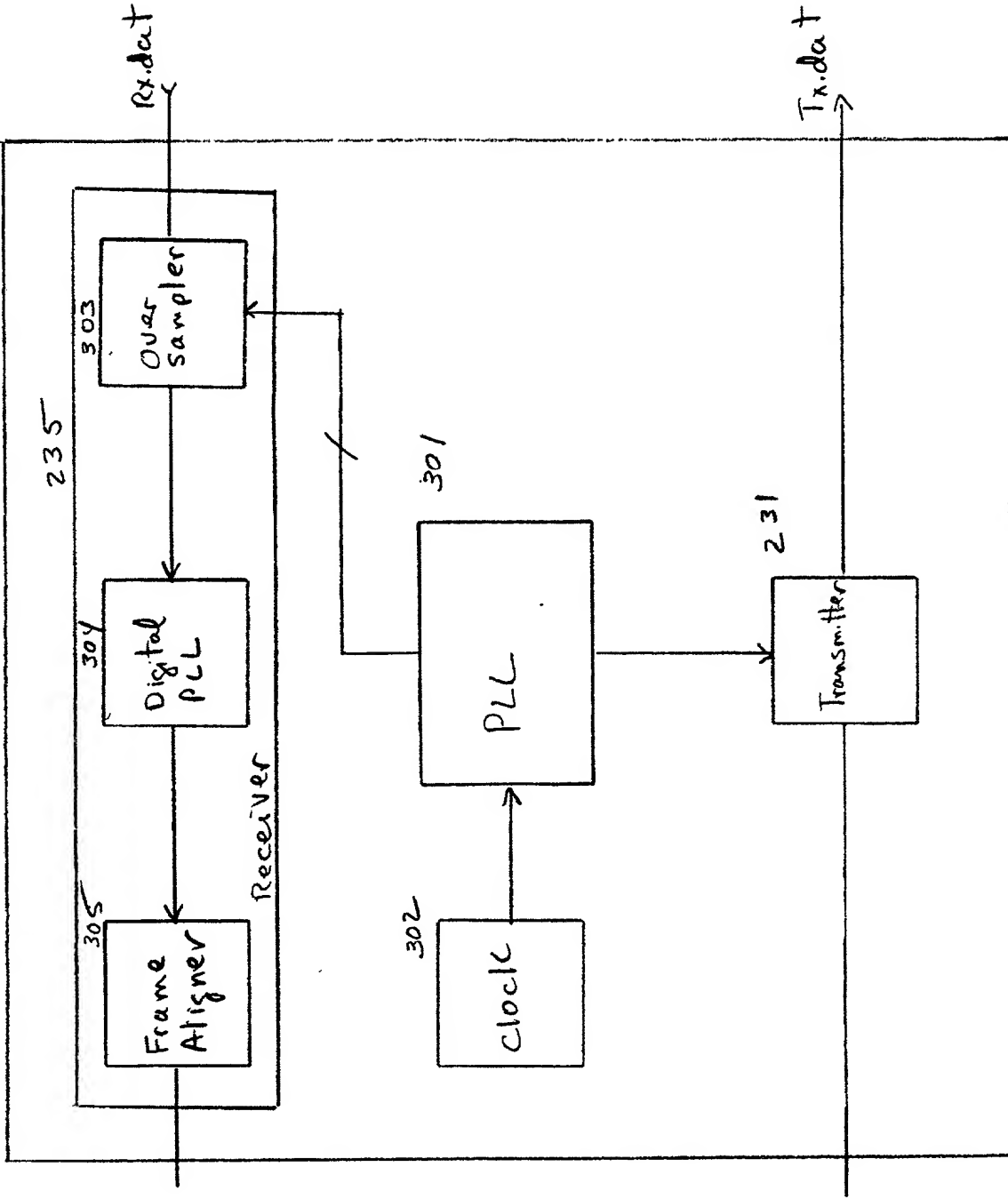


Fig 3

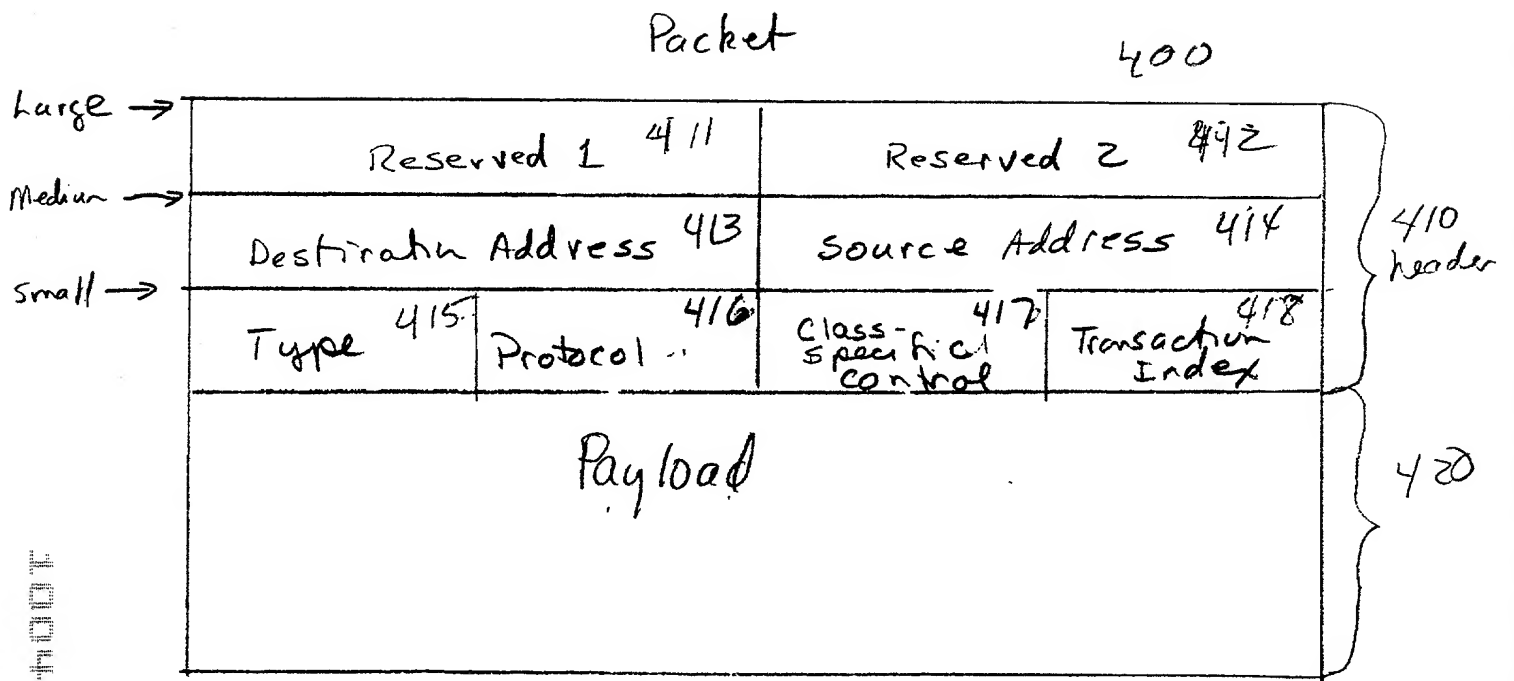


Fig 4

TO Payload Shoot

500	501	502	503	504	505	506
Header	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6

570

address 500a

520	501	502	503	504
Header	Block 1	Block 2	Block 3	Block 4

520

address 500a

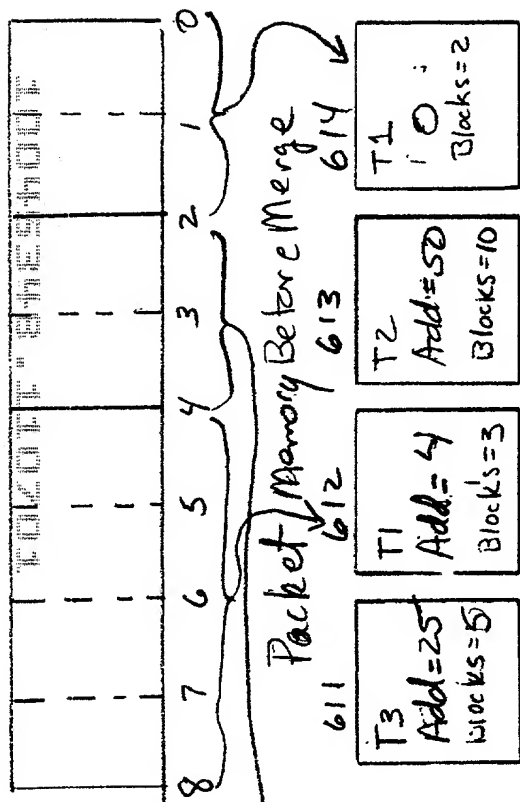
531a

531	505	506
Header	Block 5	Block 6

address + 4

F.45

600



Packet/Memory Buffer Merge

610.

212

M-1

419

T3
Add = 25
blocks = 15

TI
Add. = 4
Block's = 3

T2
Add:=SD
Blocks=10

T1
10
Blocks = 2

Received
Pack of

T1 /
 Add = 2
 Blocks = 2

630

Packet Money After Merge 613 614

029

19

II.

T3
Add=25
Blocks=5

T2
Add=50
Block=10

T1
Add=0
Blocks=7

Li
x
2

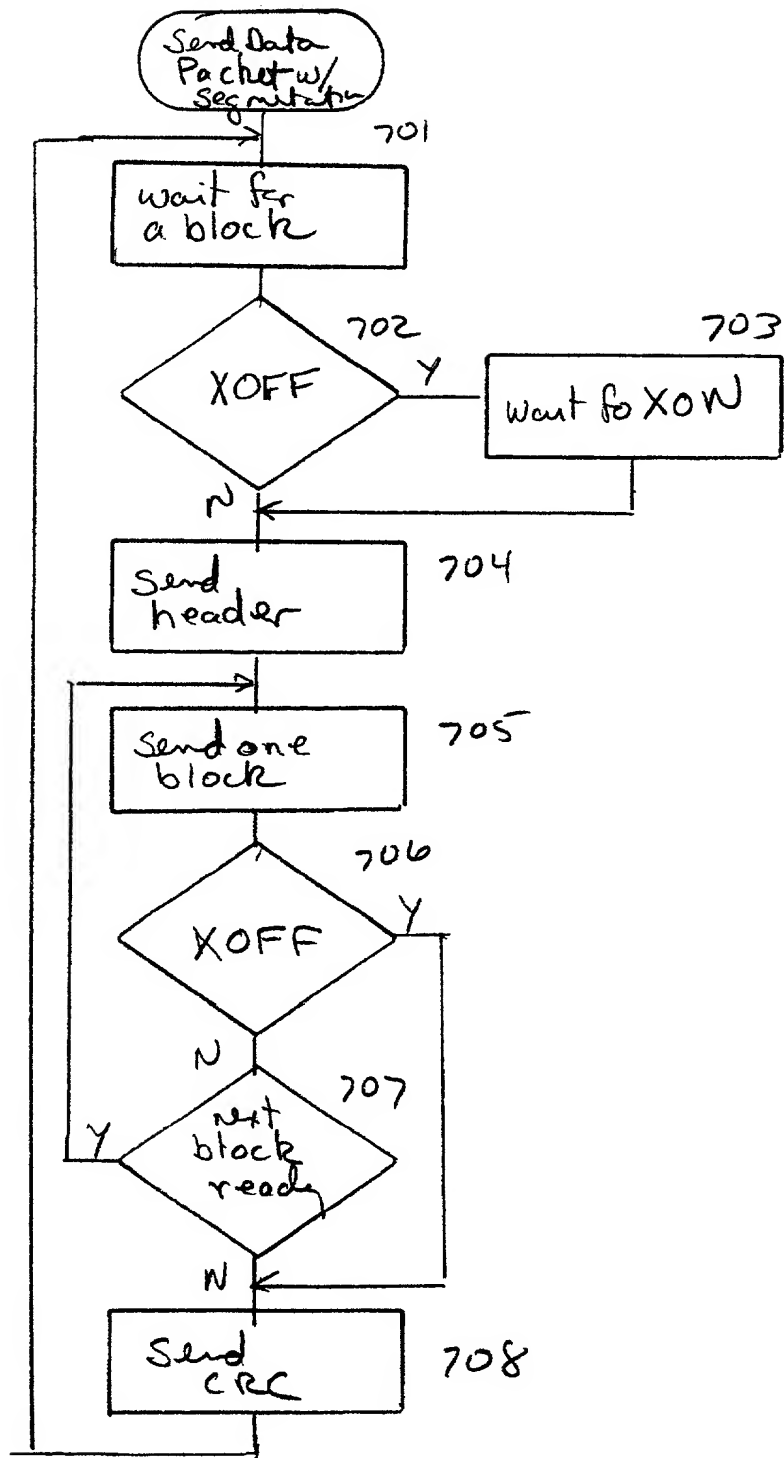
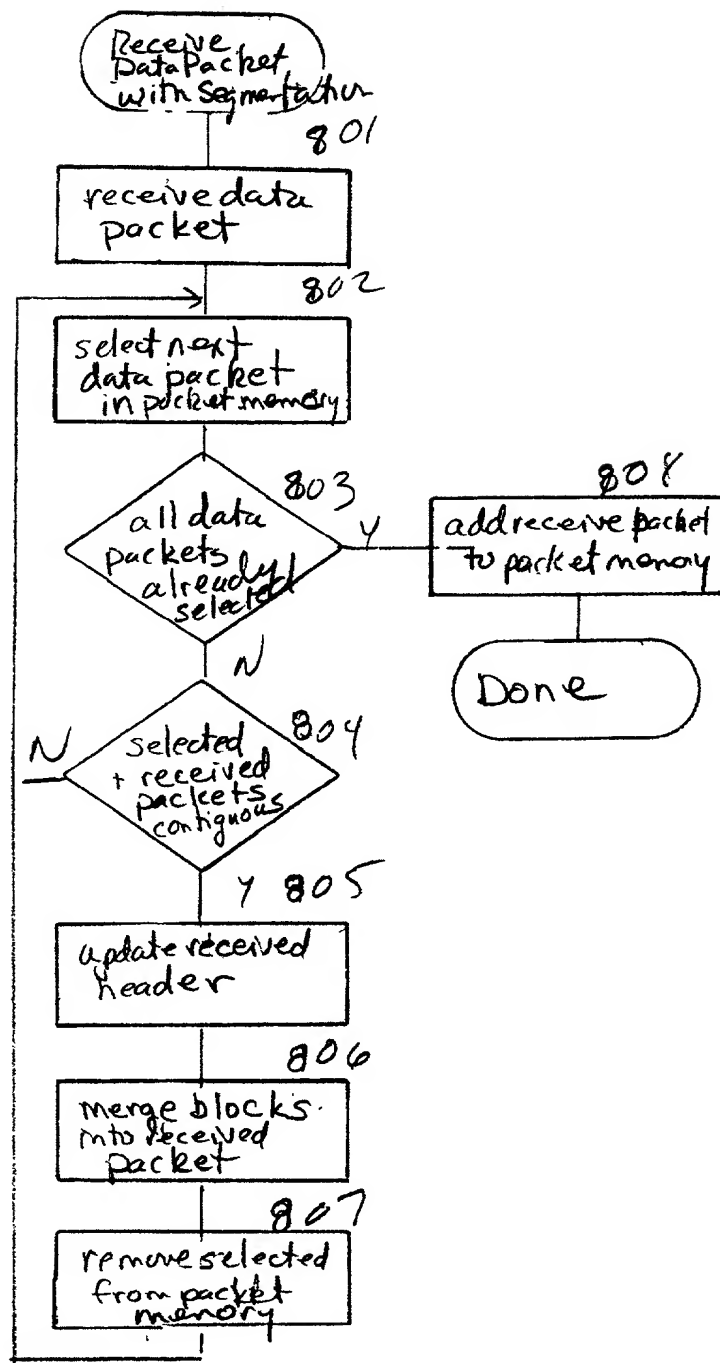


Fig 7



Fig



Sync + packet type

Fig 9A

		A8	A7	A6	A5	A4	A3	A2	A1	A0	B8	B7	B6	B5	B4	B3	B2	B1	C0	C8	C7	C6	C5	C4	C3	C2	C1	C0
BIT BUFFER																												
BIT CONTENT		0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0
"10" DETECTION		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
"10" DETECTION		0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
RESULT																												
Symbol																												
STARTING																												
POINTS																												

FIG.10

Fig 9B

910

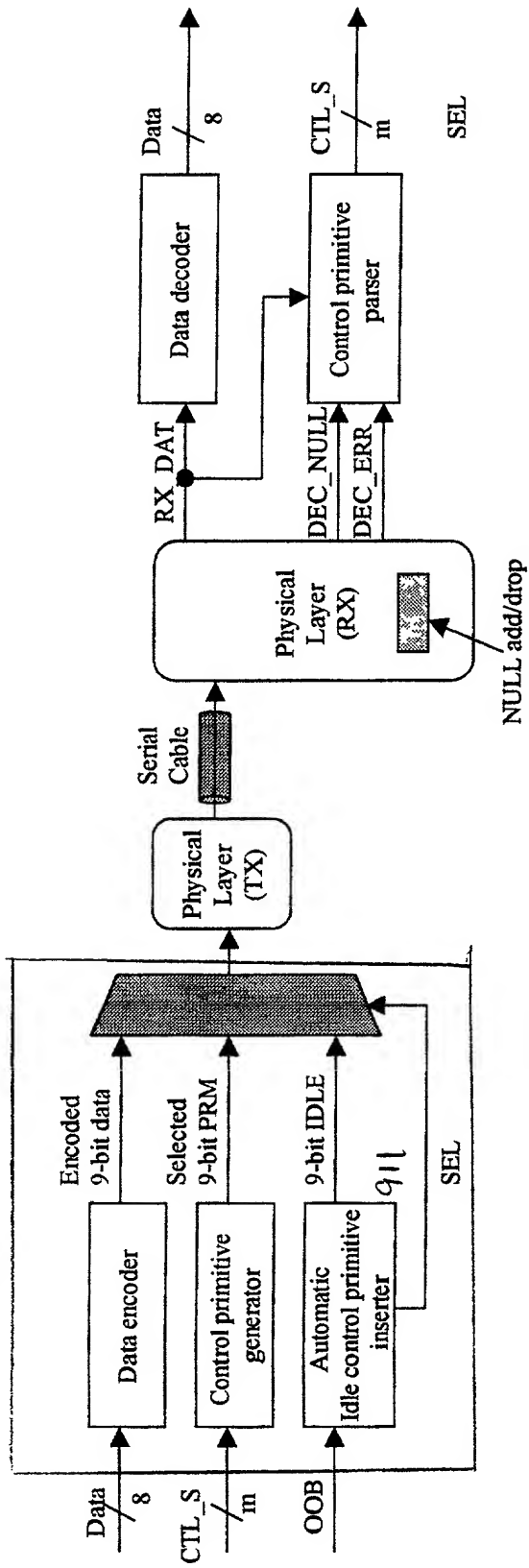


Fig. 9C

FIG. 9C

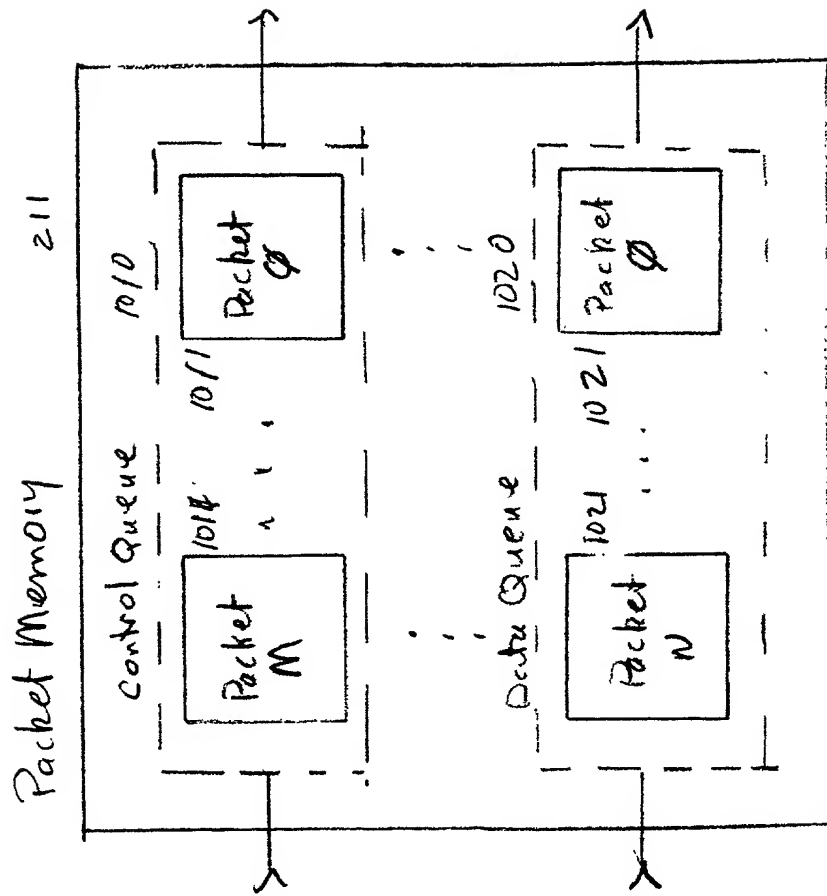


FIG. 10

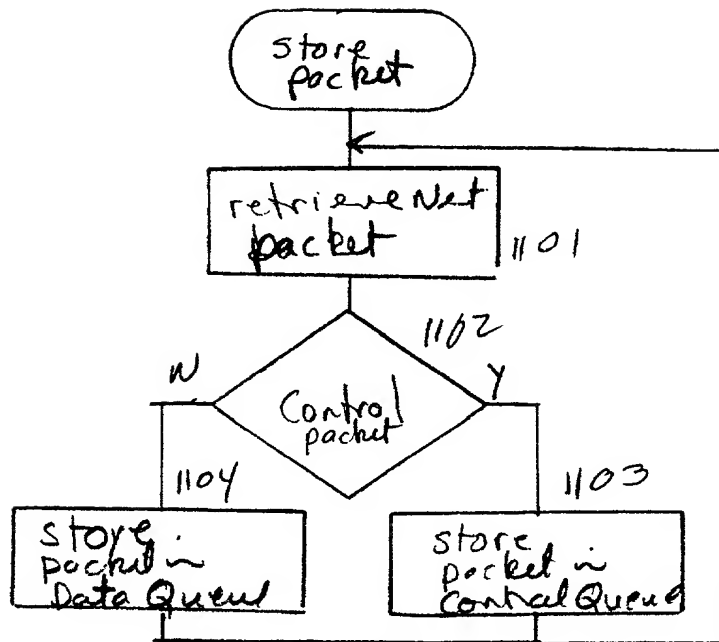


Fig 11

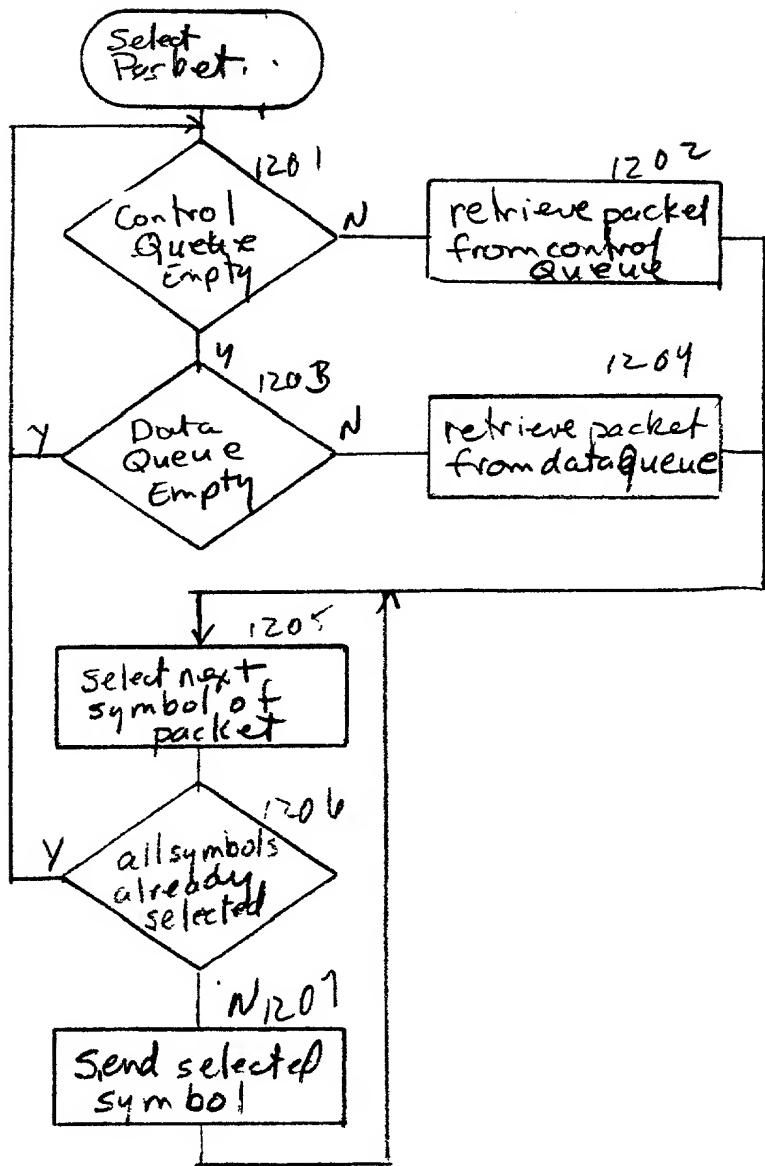


Fig 12

TOGETHER SHOOT

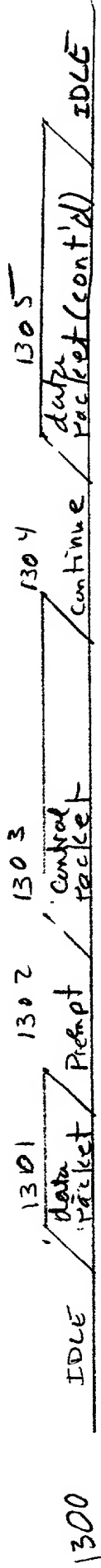


Fig 13

FIG. 10

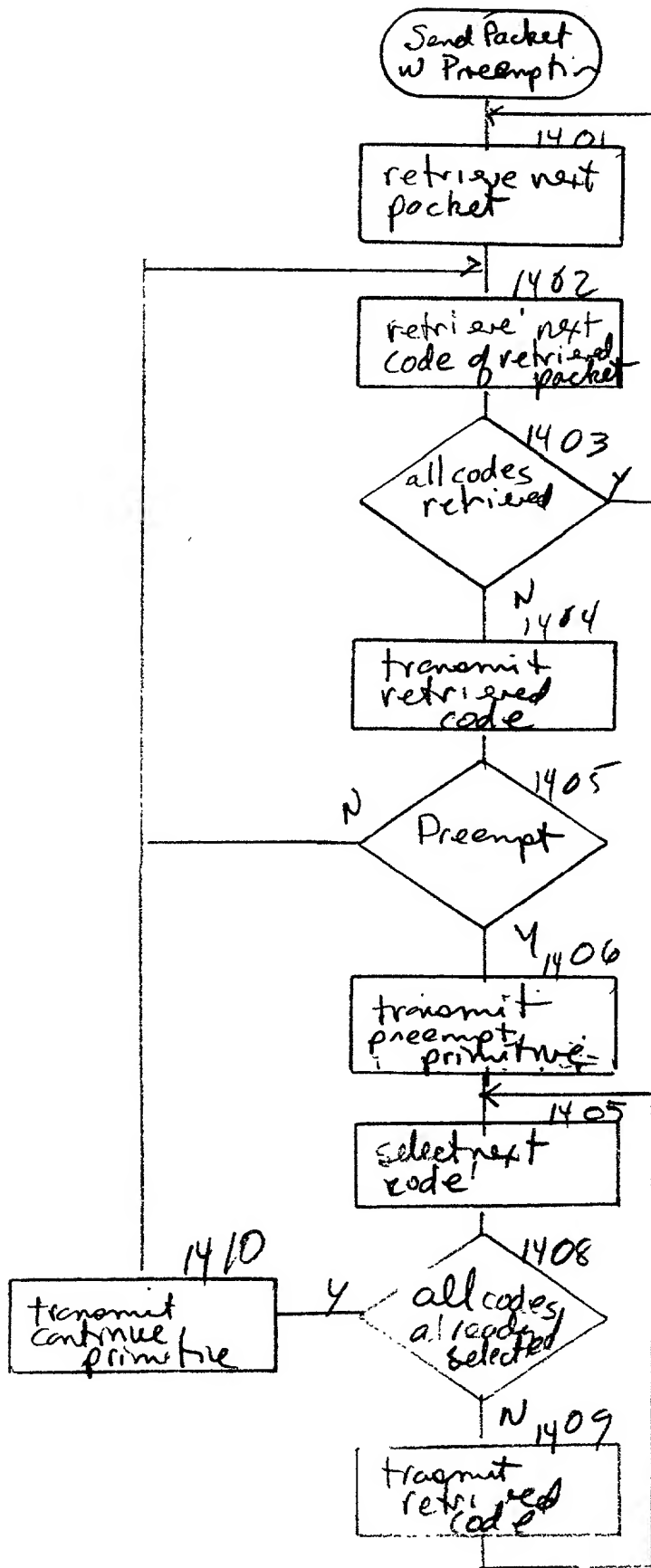


Fig 14

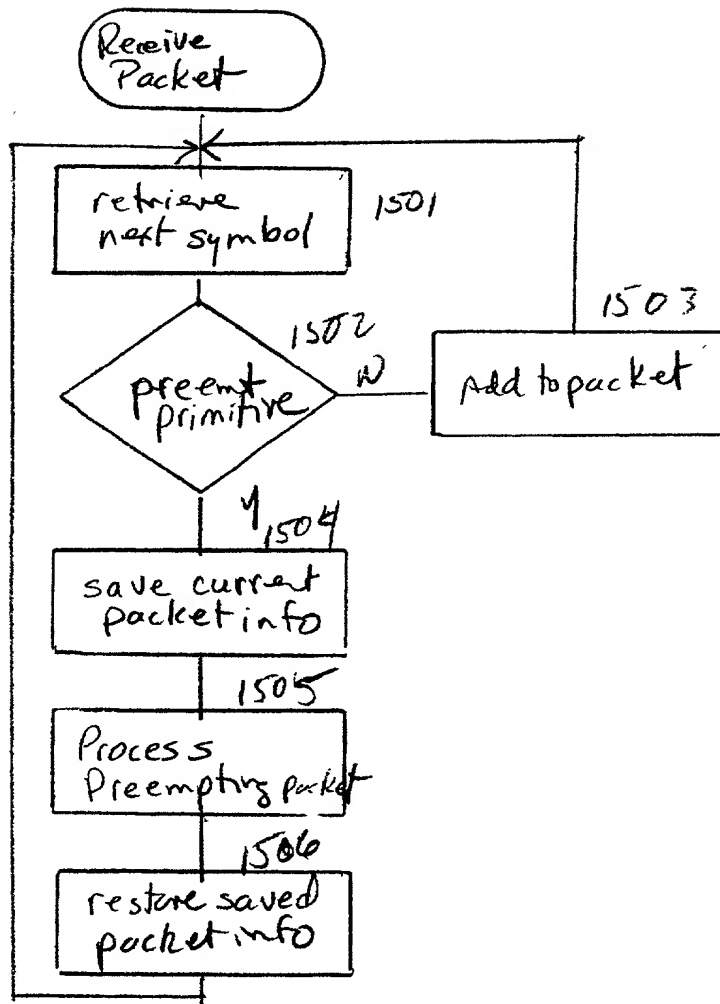


Fig 15

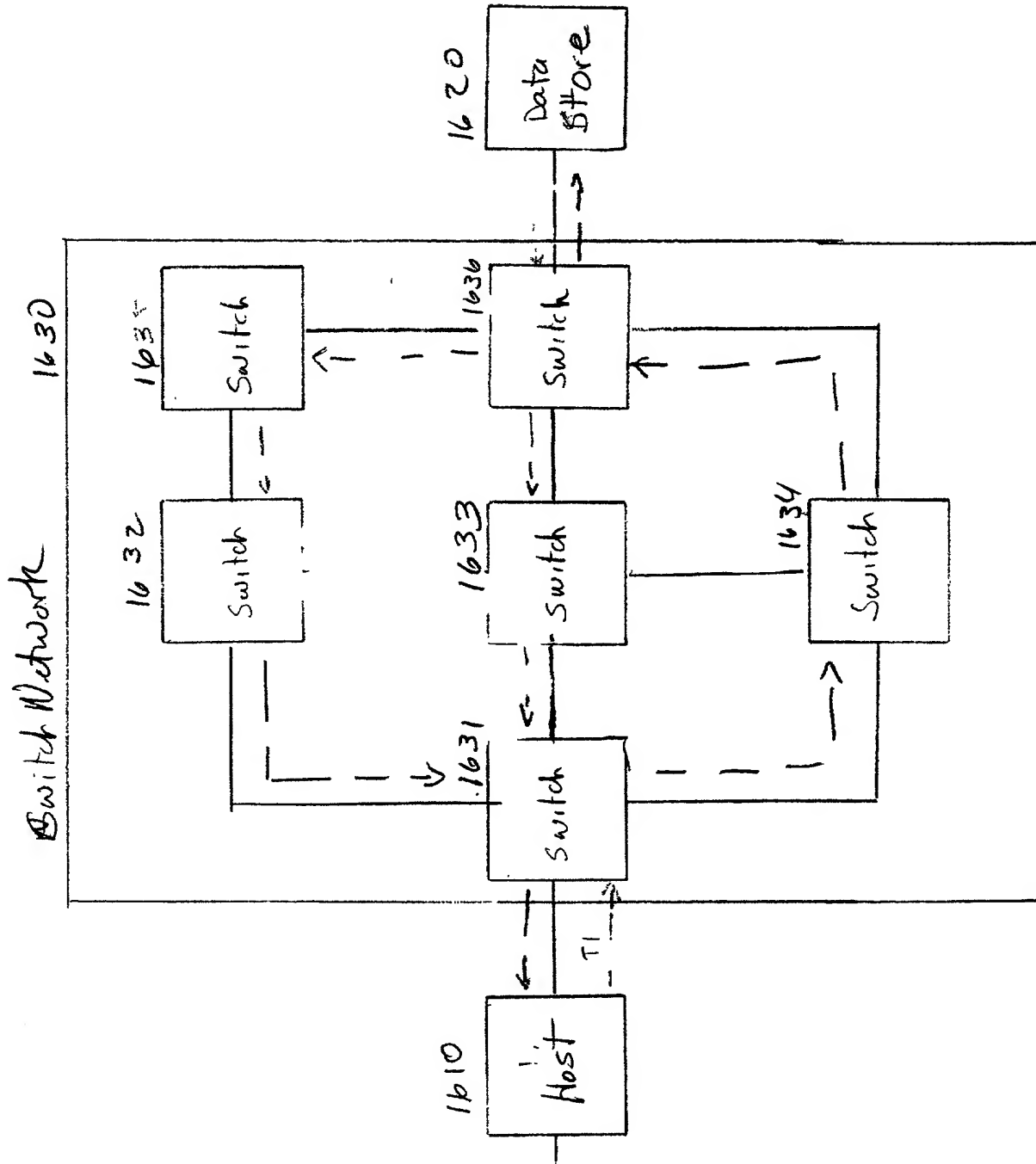
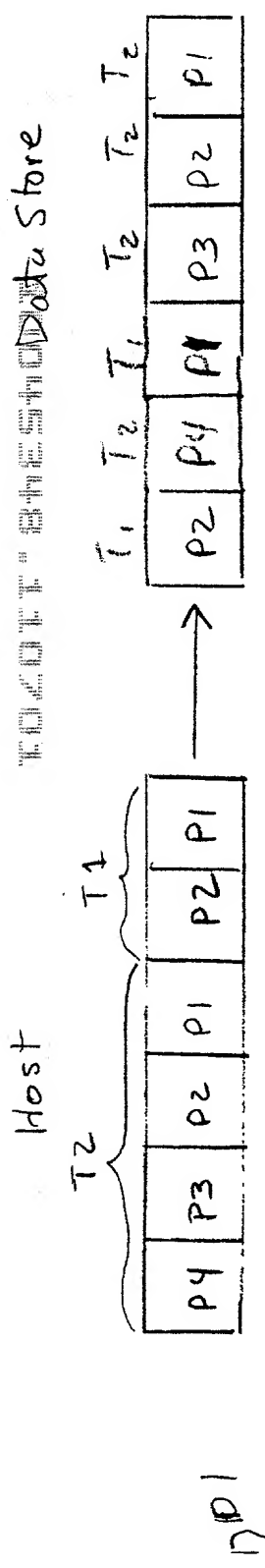
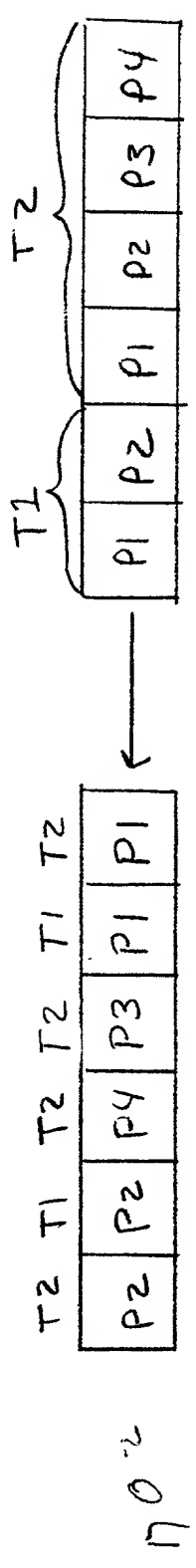


Fig 16

LOCAL BUFFER Data Store



Preserving Packet Order w/ Transaction



No Packet or Transaction Ordering

Fig 17

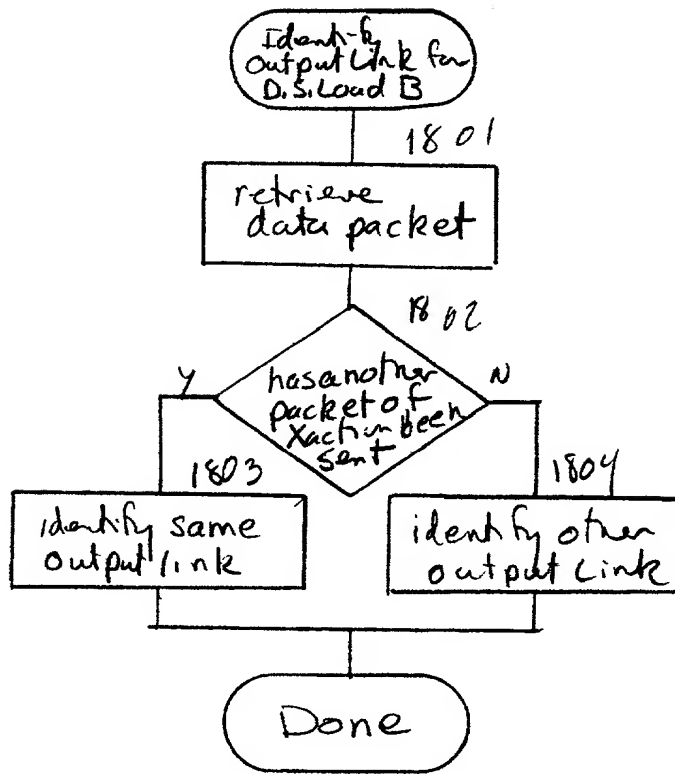


Fig 18

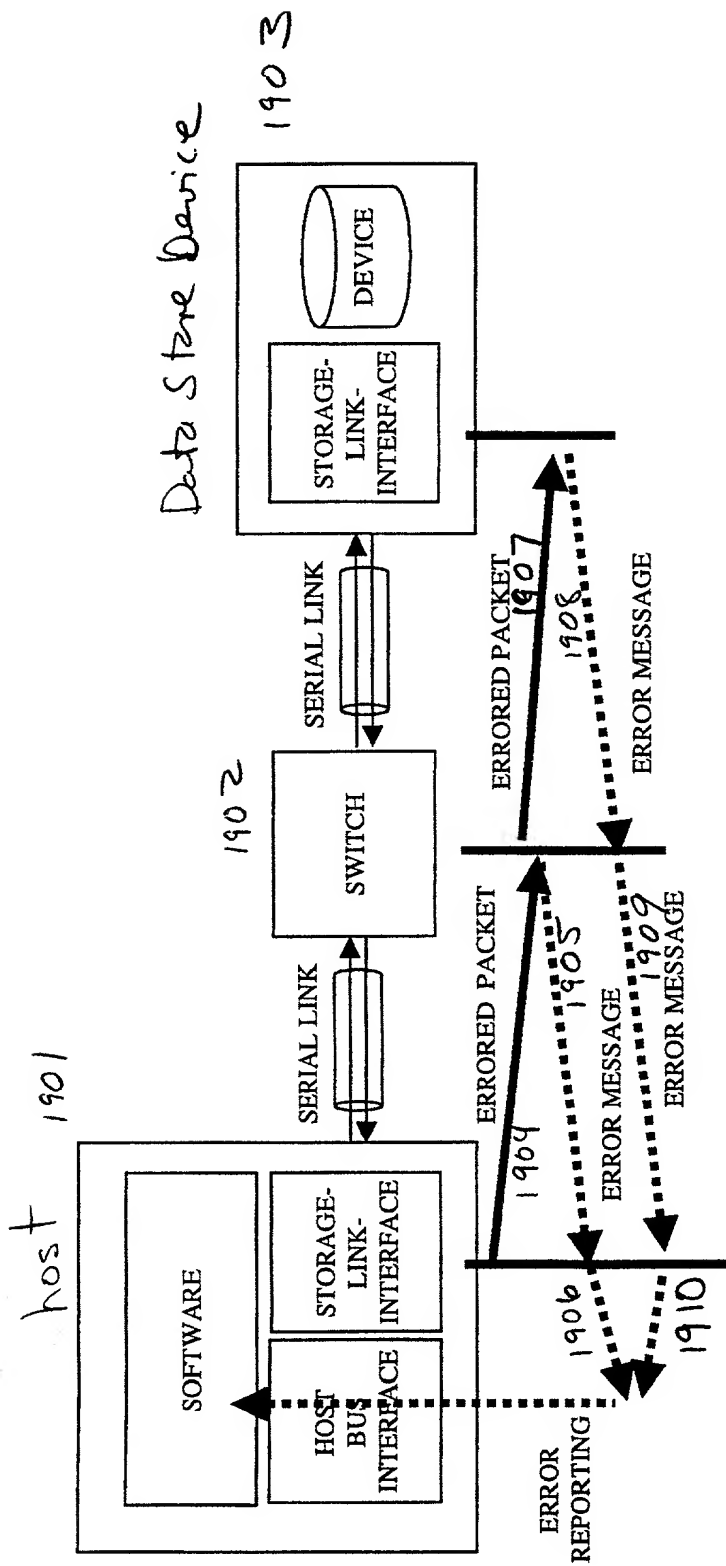


Fig 19A

1901A

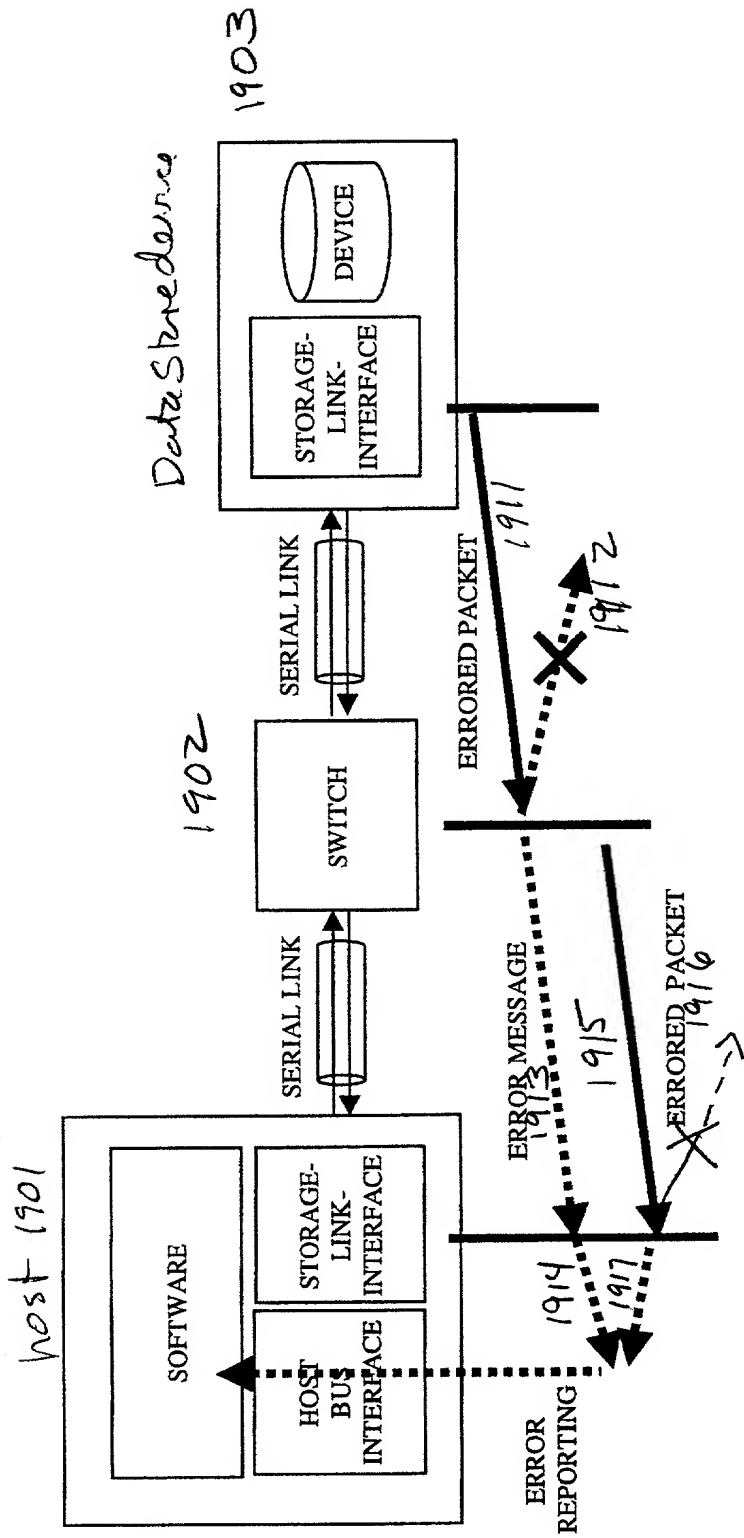
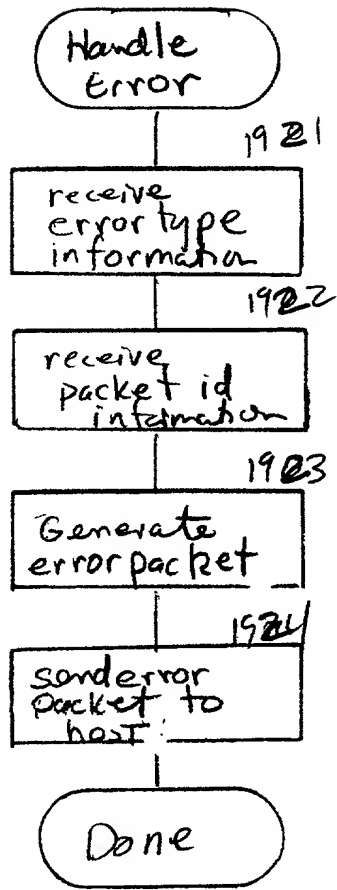


Fig 19B



19C

8b Code	9 bit symbol
0000 0000	101010101
0000 0001	101010100
0000 0010	101010111
⋮	
0101 0101	001010101
⋮	
0111 0110	001110110
0111 0111	100100010
⋮	
1111 1111	110101010

Fig 20

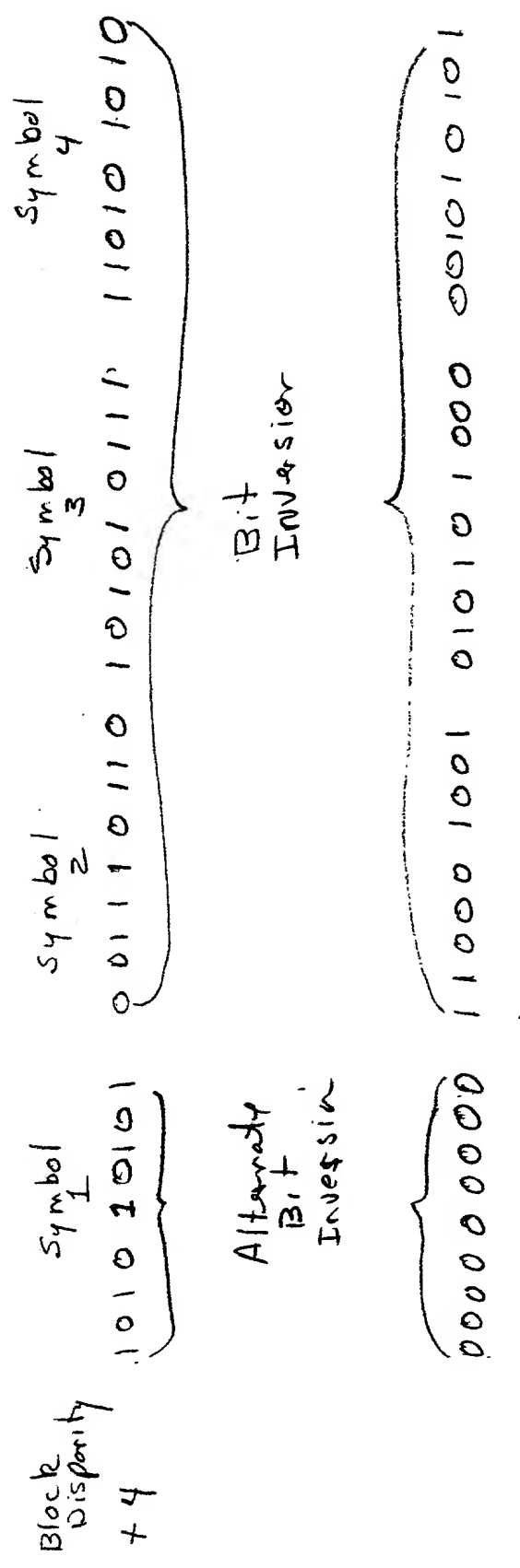


Fig 21A

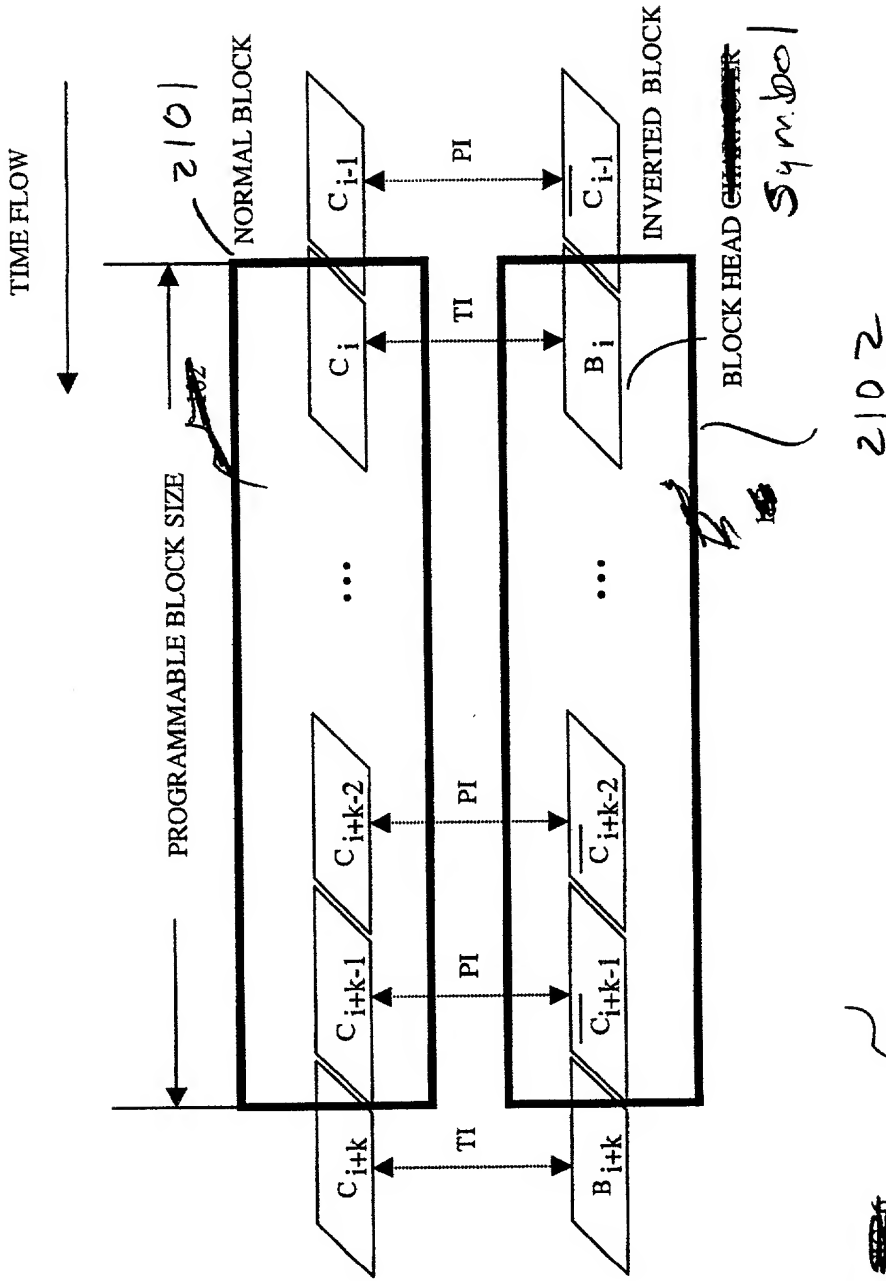


Fig 21B

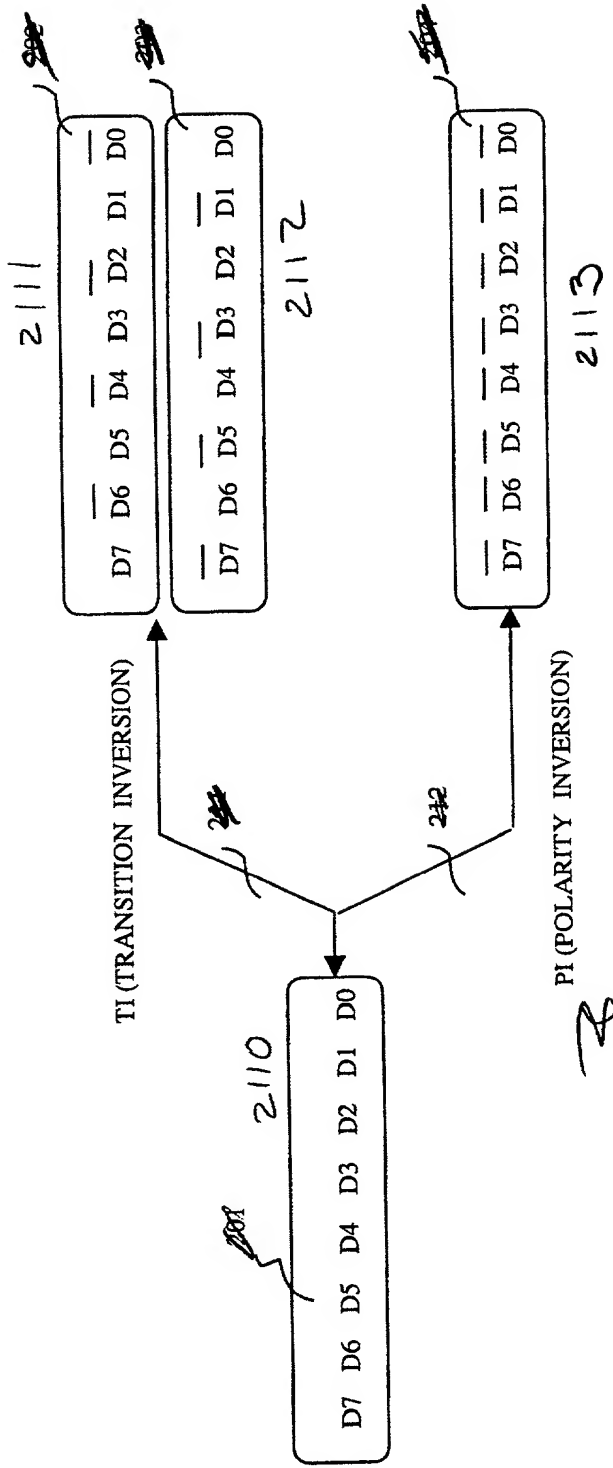


Fig 21C

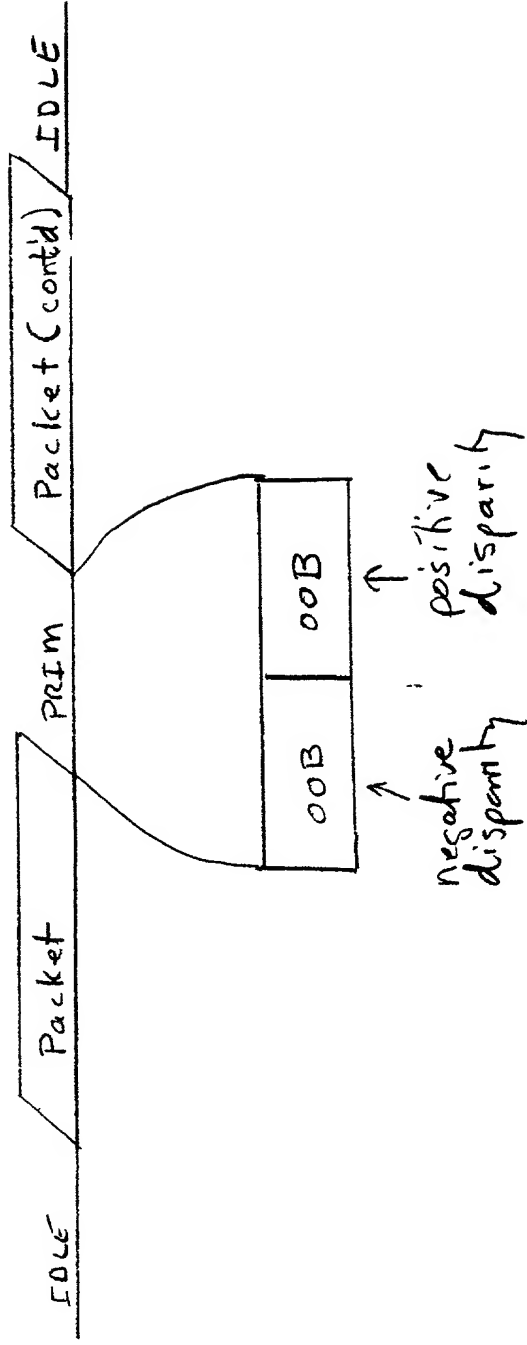


Fig 22

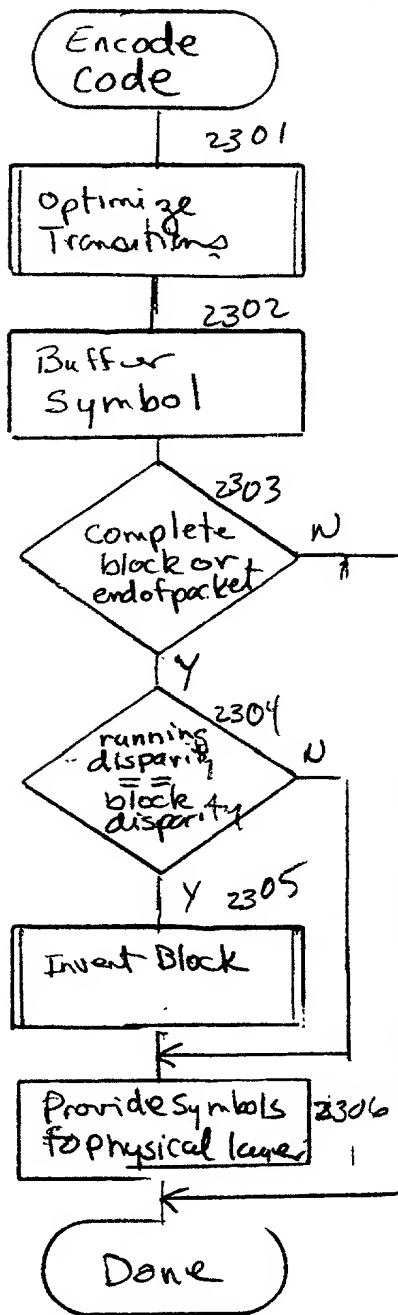


Fig 23

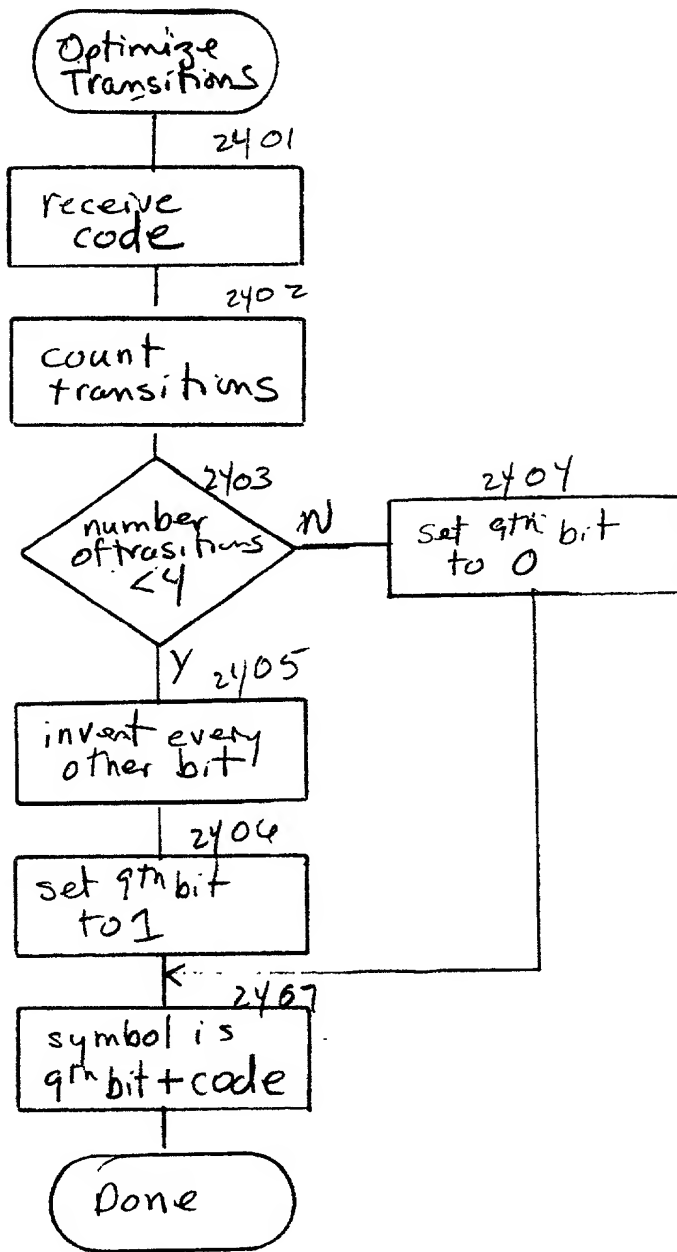


Fig 24

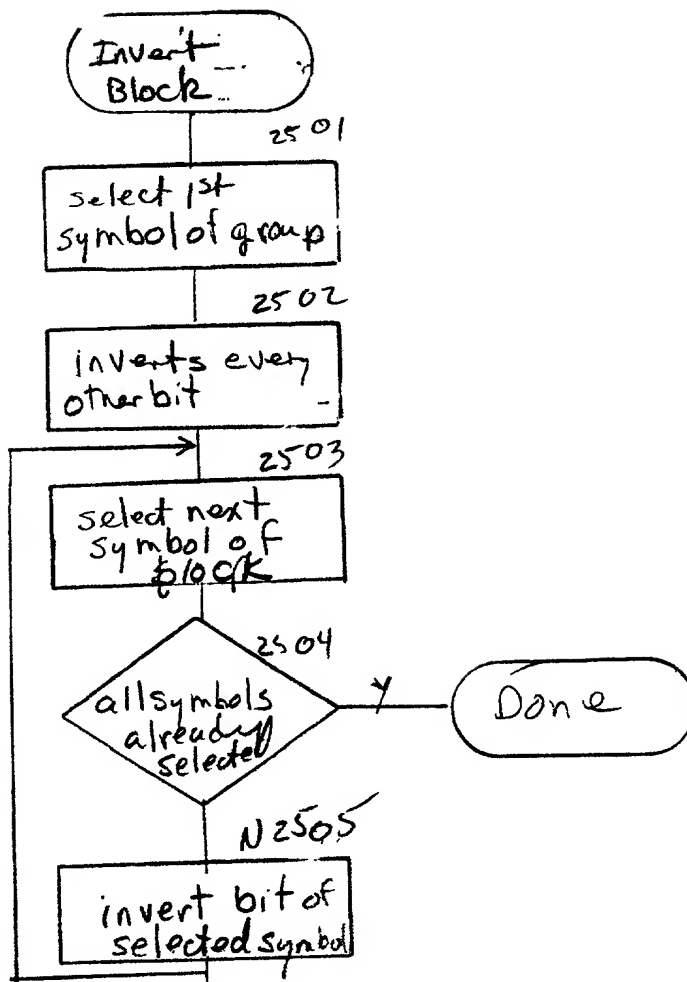


Fig 25

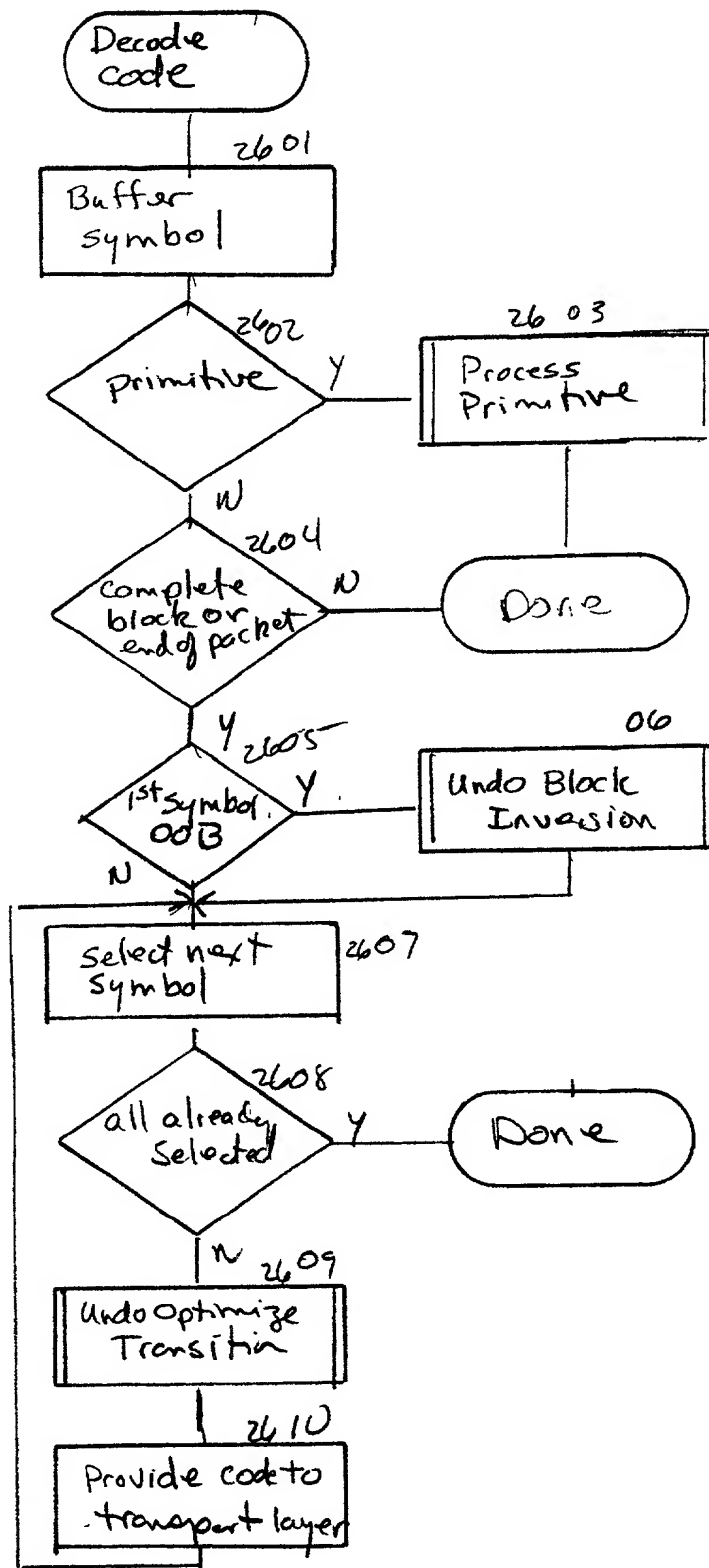


Fig 26

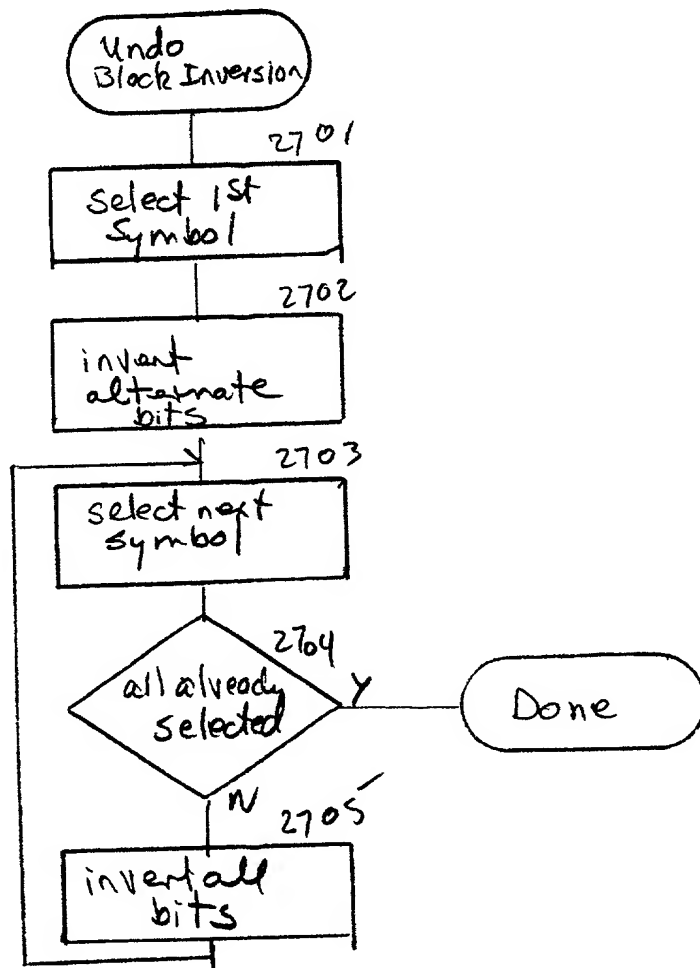


Fig 27

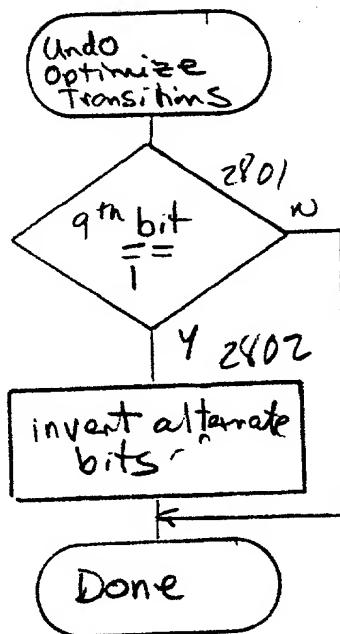


Fig 28

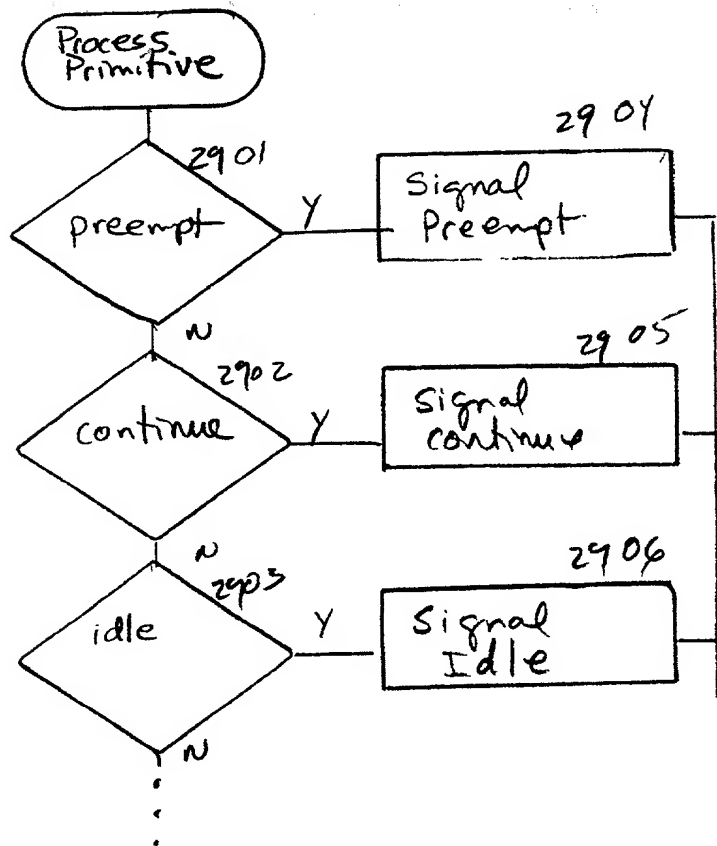


Fig 29

Multipoint Memory Device 3000

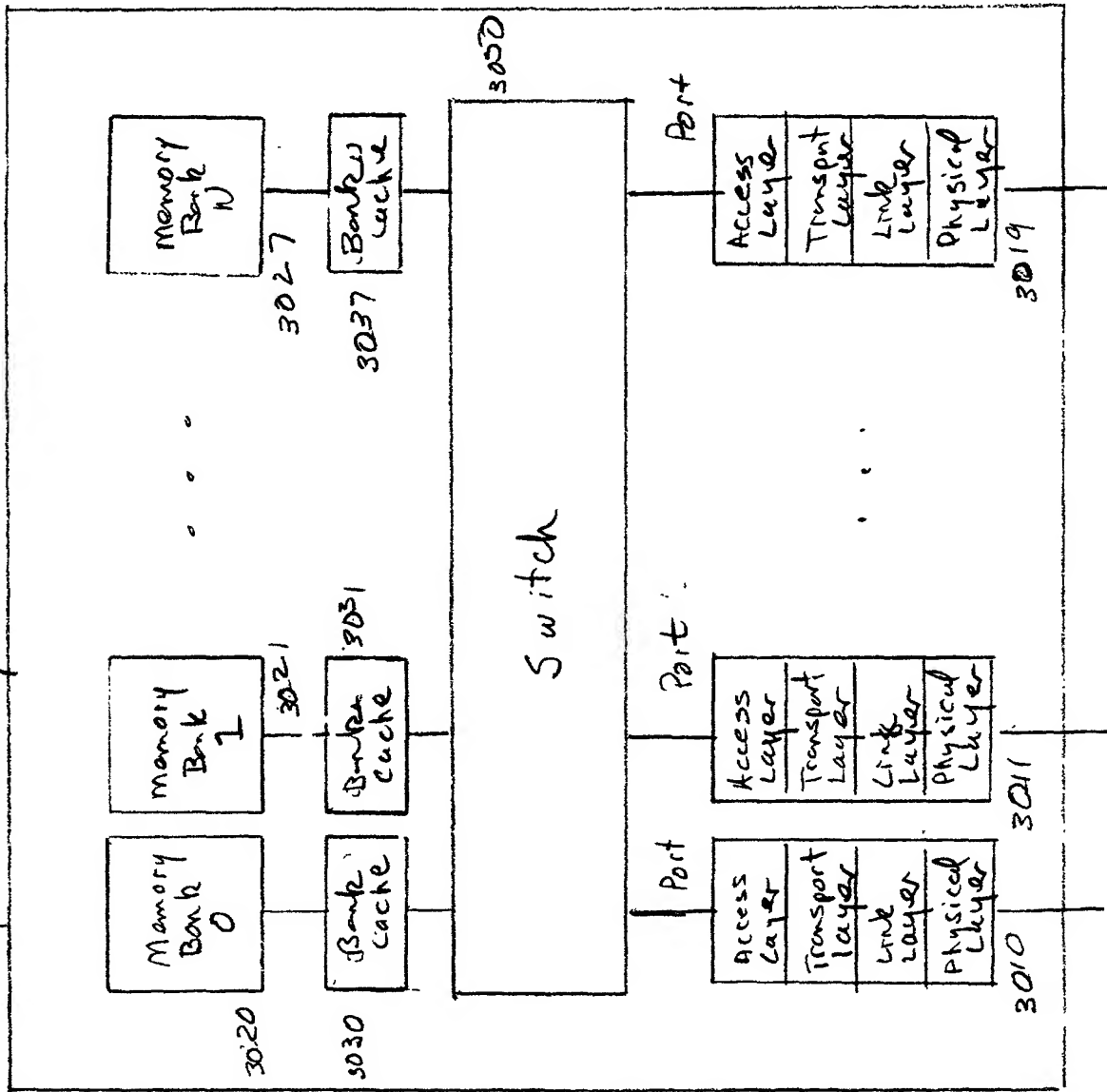


Fig 30

Input Queue 3201

Port	R/W	Address	Data
3	R	1000	
4	W	4000	10...1
3	W	1000	111...0
3	R	2000	
...			

Output Queue 3202

Valid	Port	Data
1	3	11...0
0		
0		
1	3	101...1
...		

Fig 32

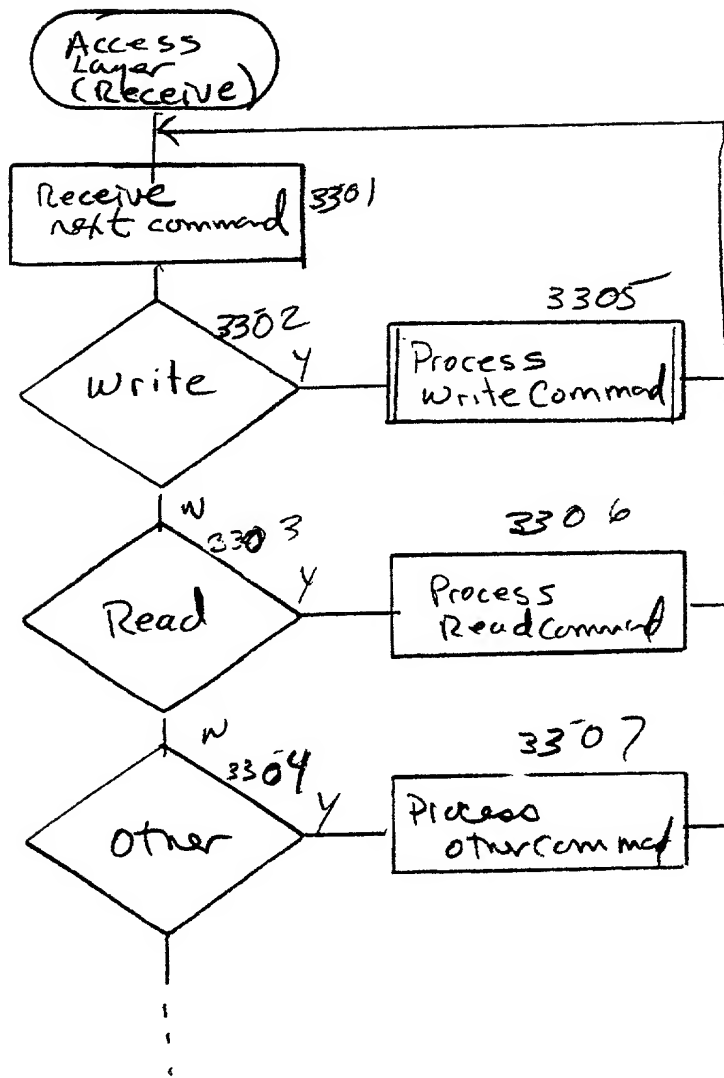


Fig 33

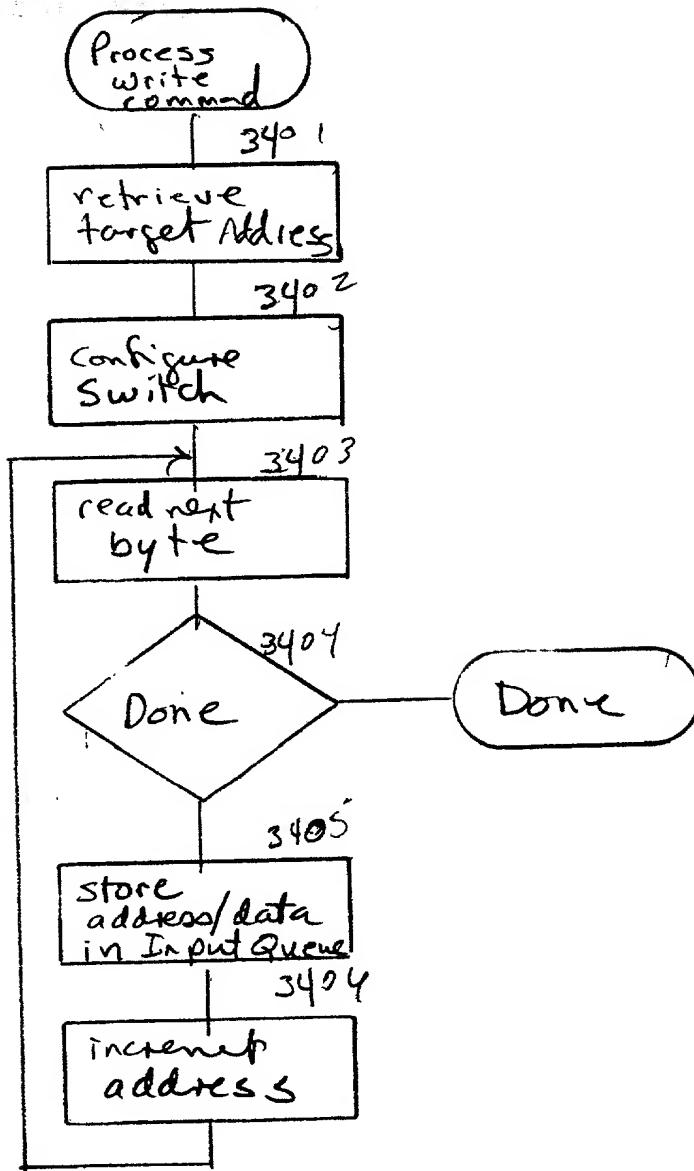


Fig 34

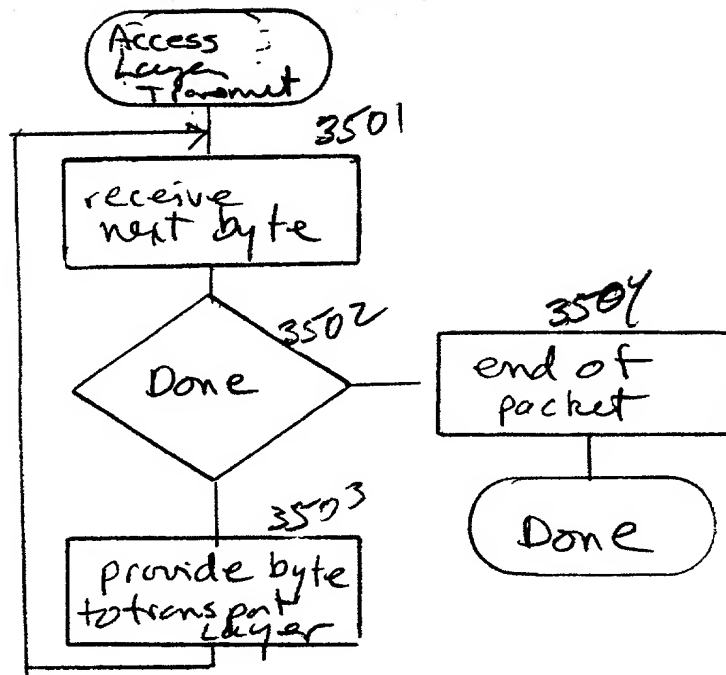


Fig 35

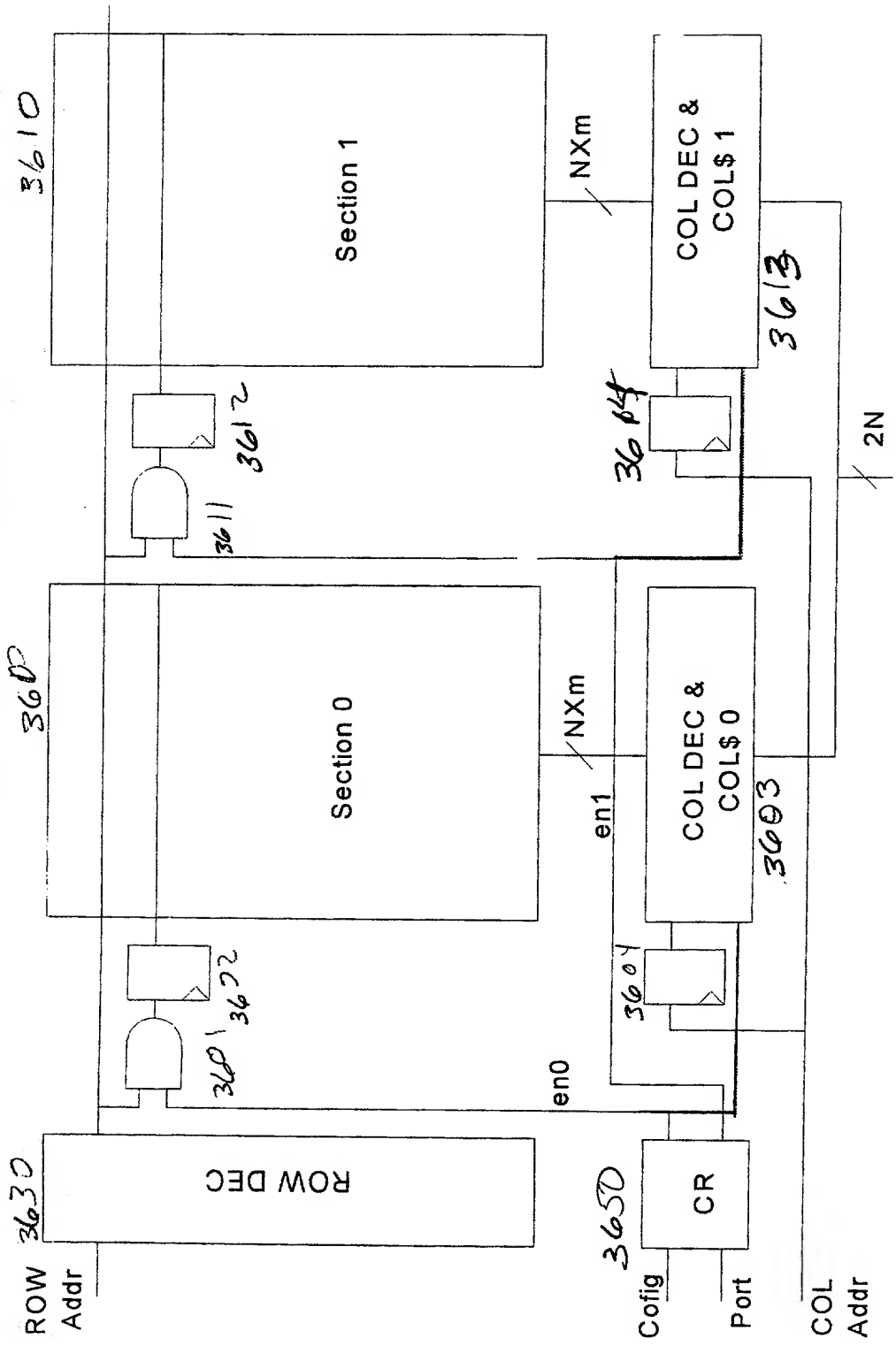
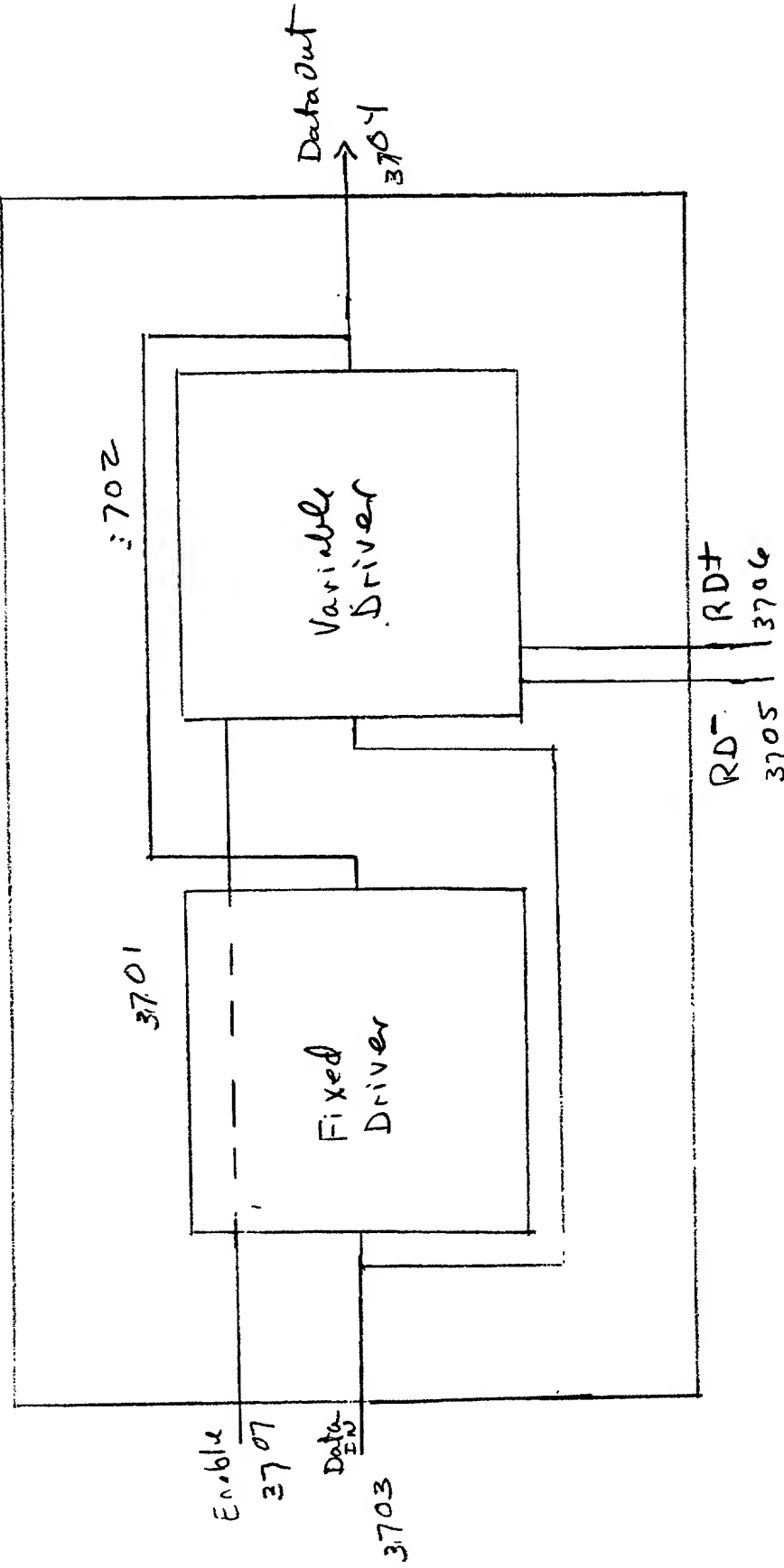


Fig 36

Line Driver 3700



Variable Driver

$\begin{cases} RD^+ \wedge DataIn = \text{pull down} \\ RD^- \wedge DataIn = \text{pull up} \end{cases}$

Fig 37A

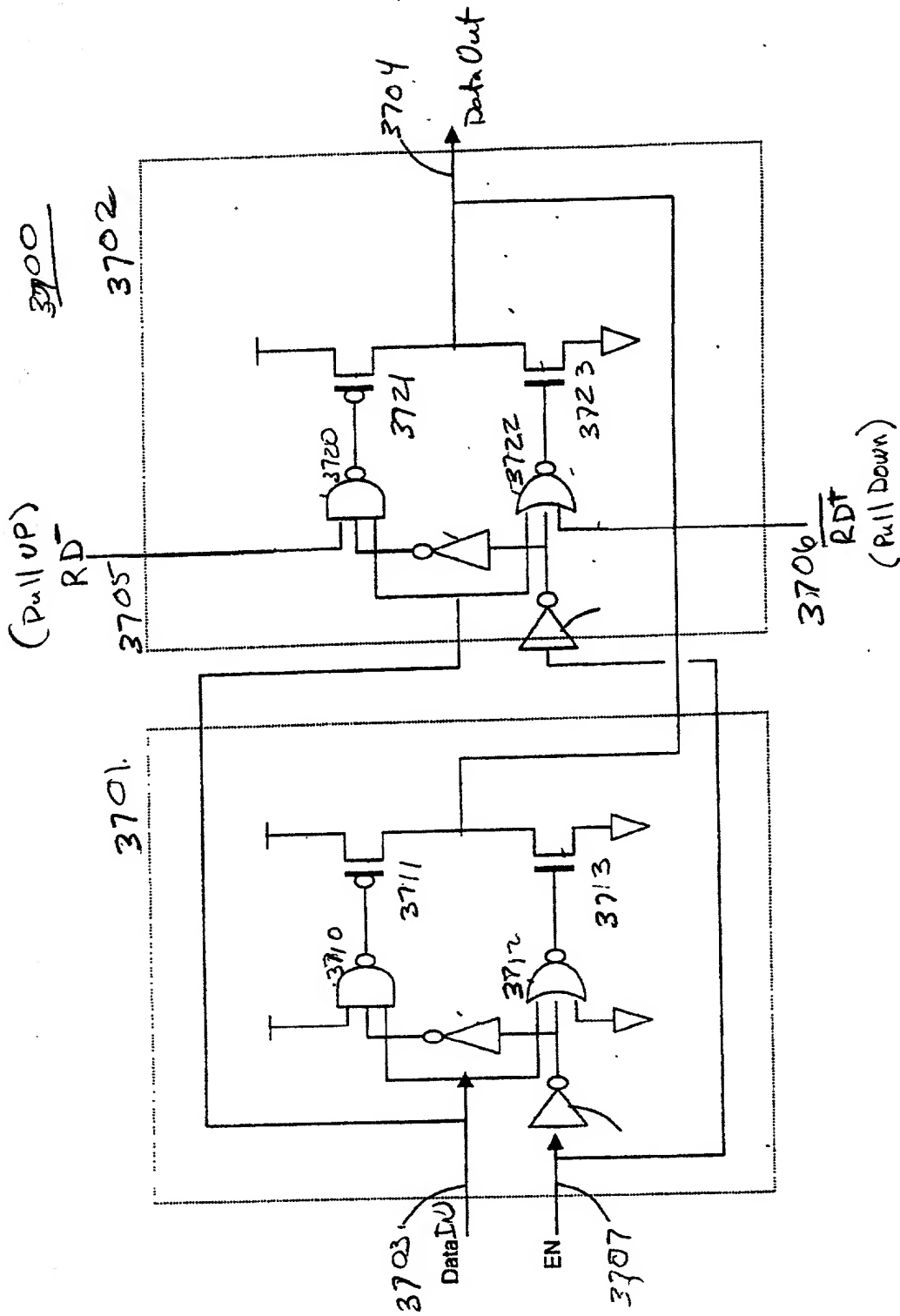


Fig. 37B

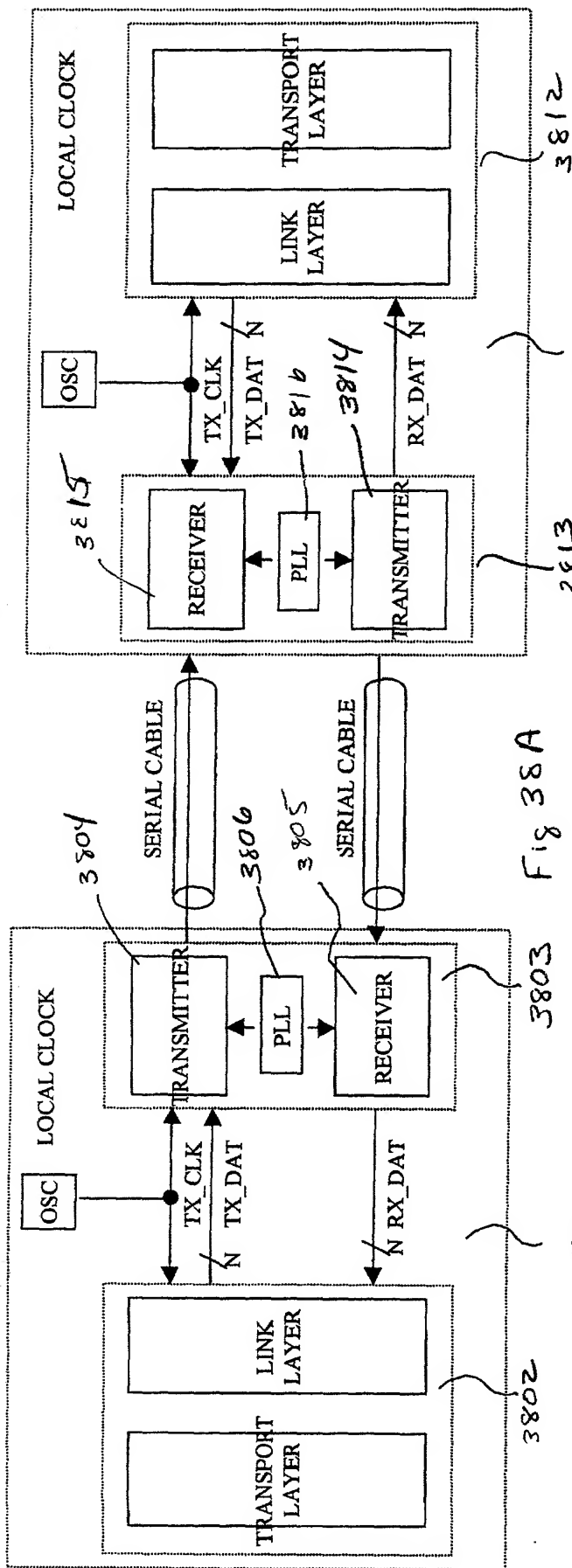


Fig 38A

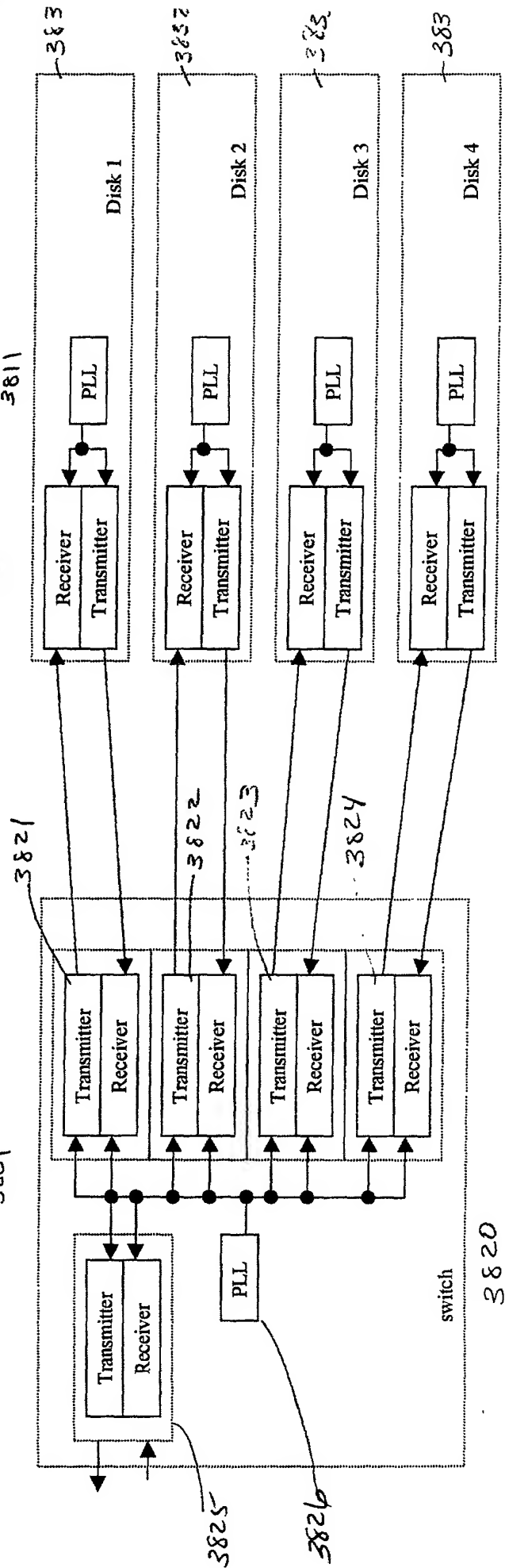


Fig 38B

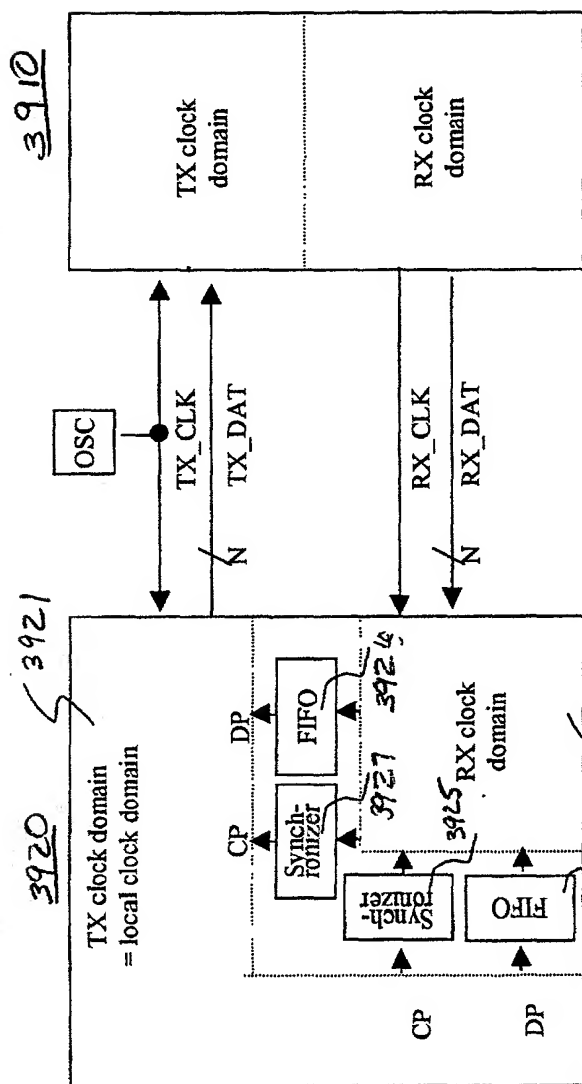


Fig 39A

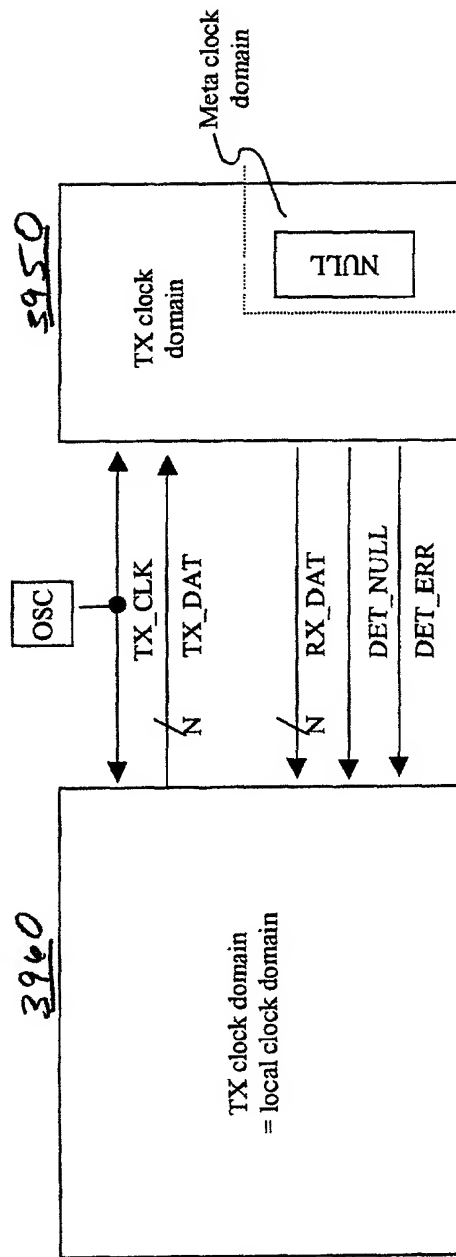


Fig 39B

FIG. 40

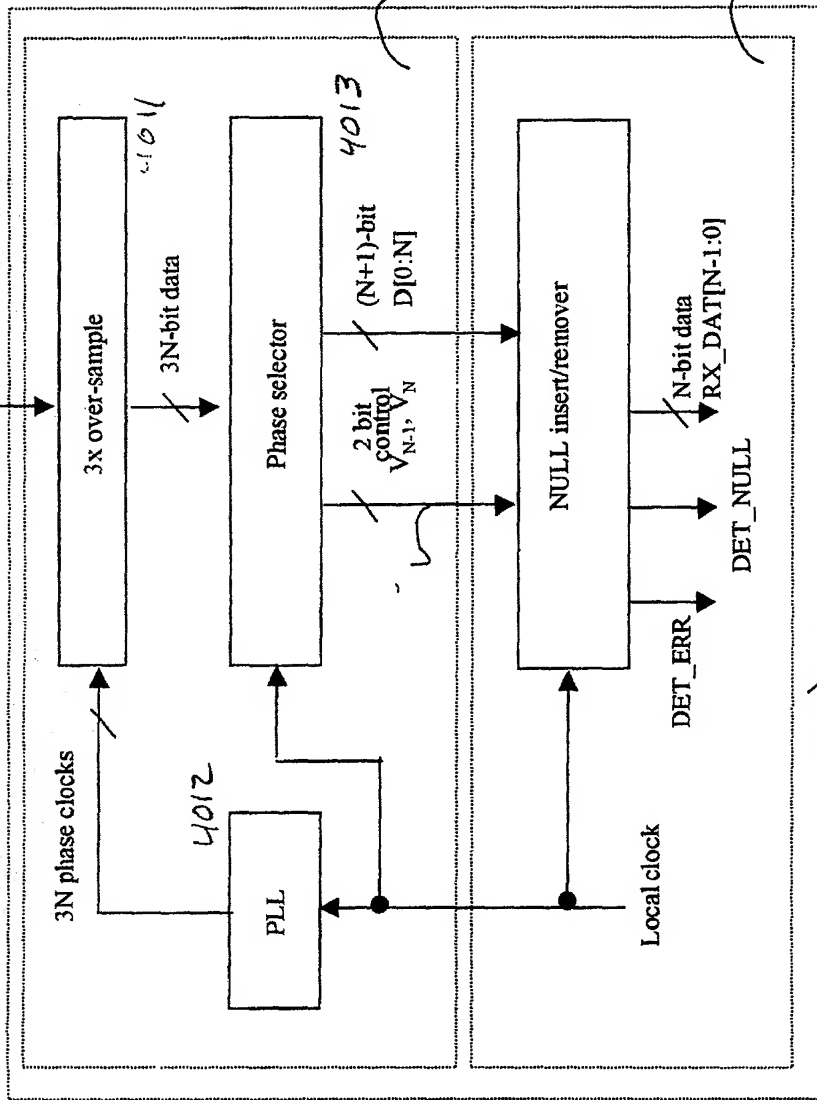


Fig 40

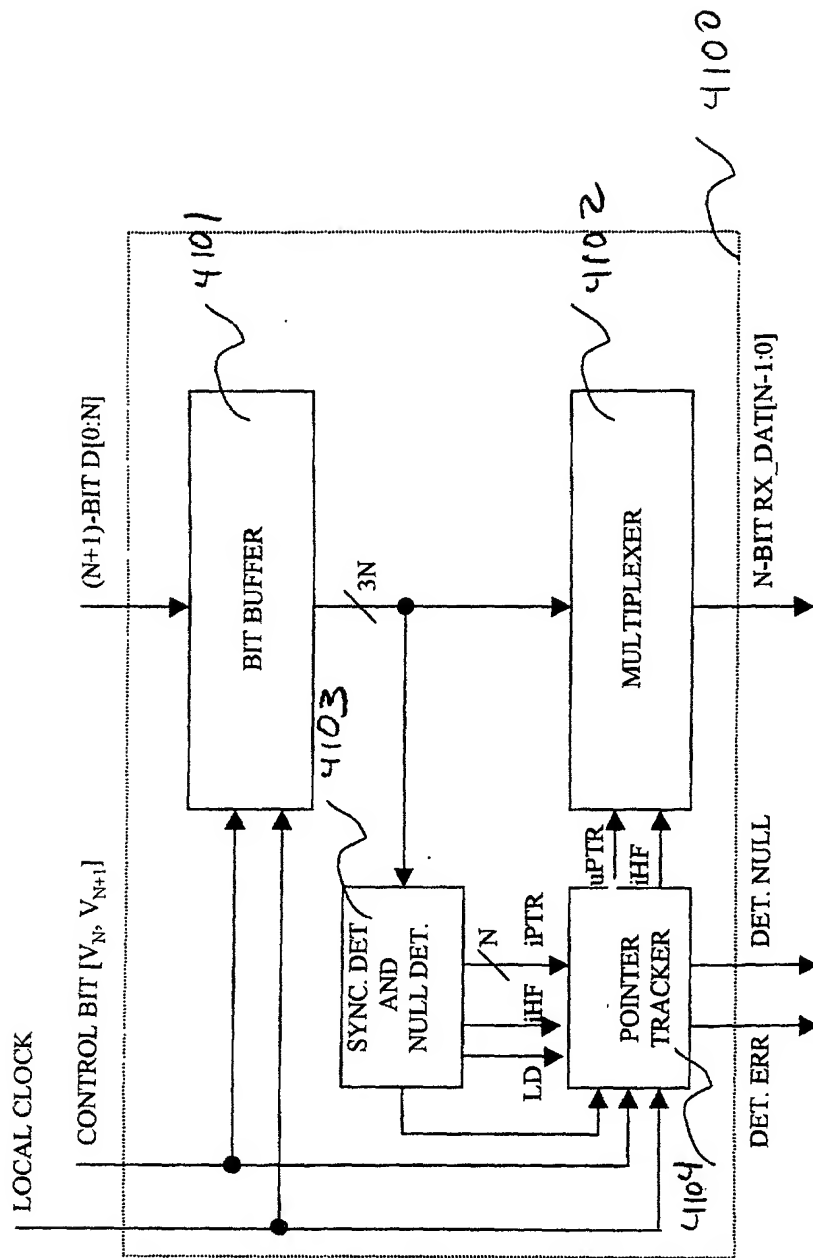


Fig 41

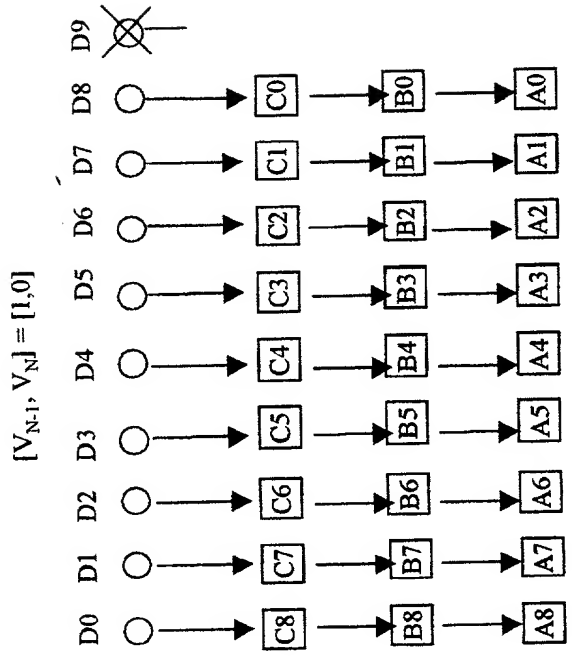


Fig 42A

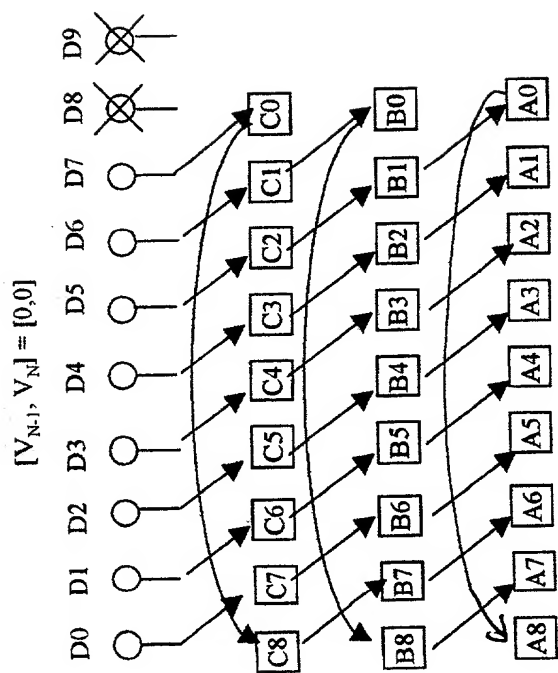


Fig 42B

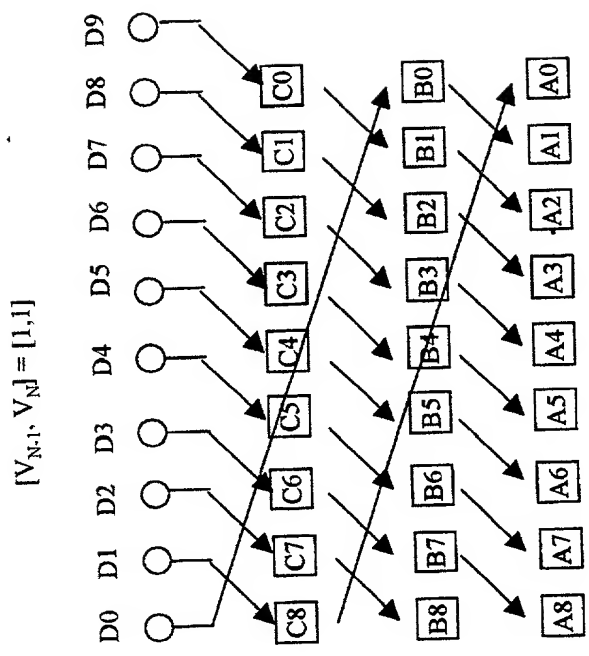


Fig 42C

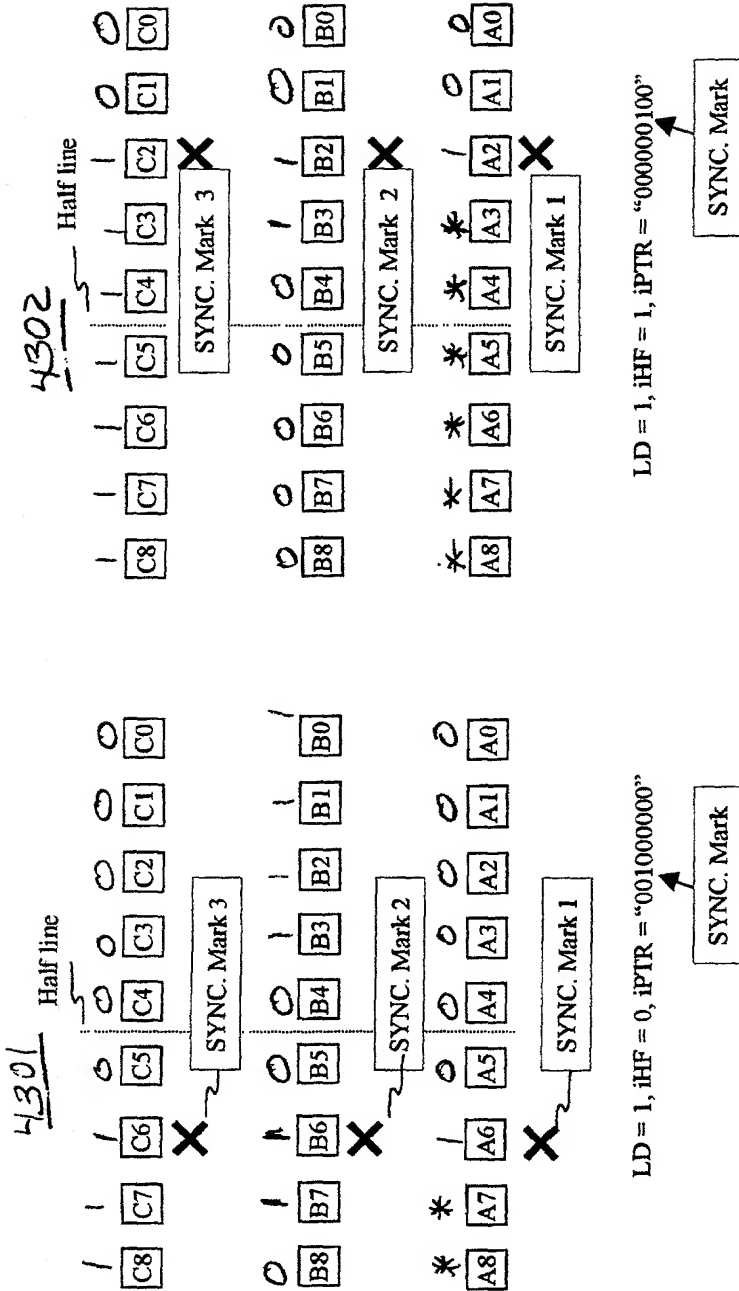
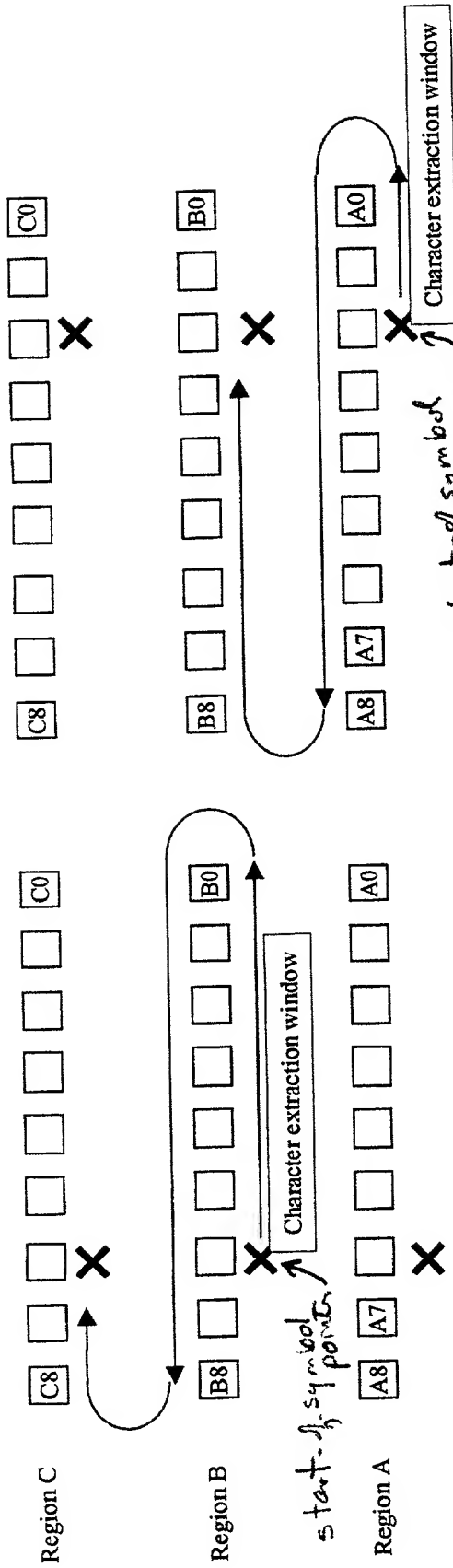


Fig. 43



LD = 1, iHF = 0, iPTR = "001000000"

LD = 1, iHF = 1, iPTR = "000000100"

Fig 44

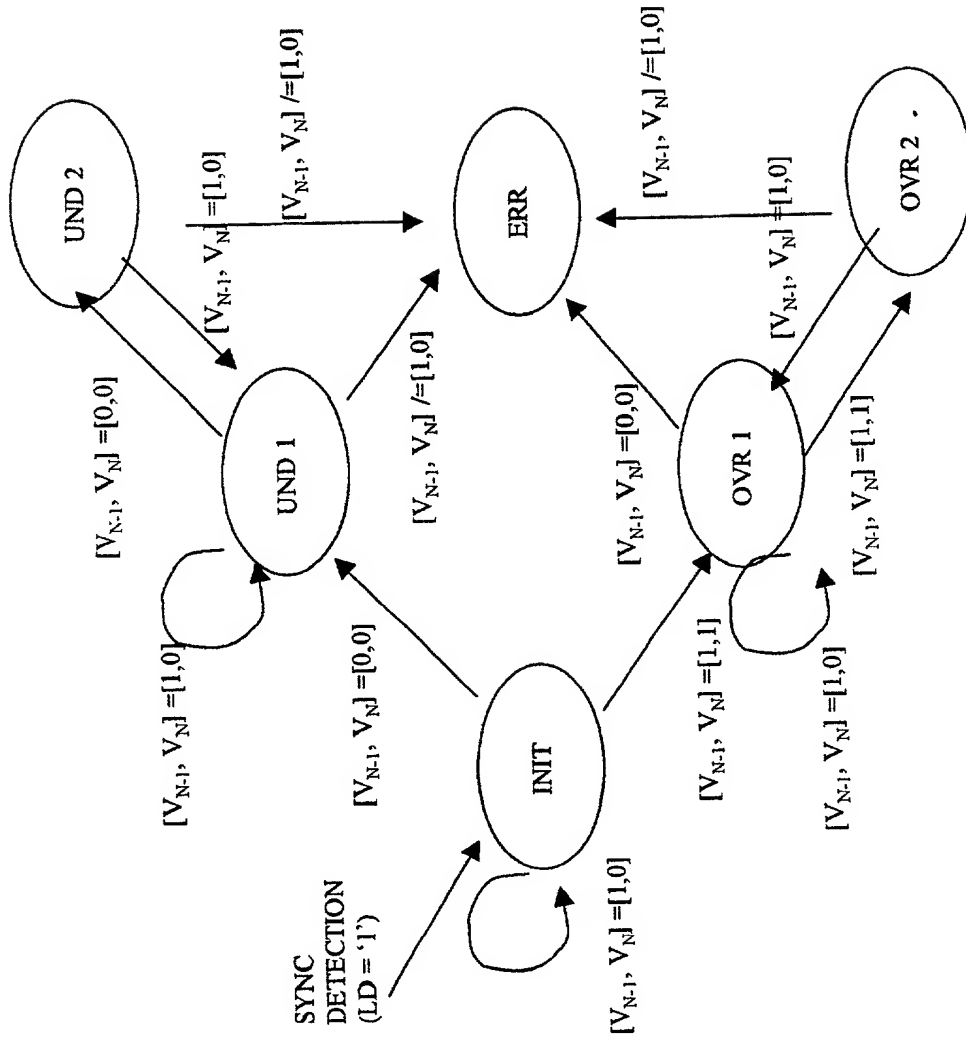


Fig 45

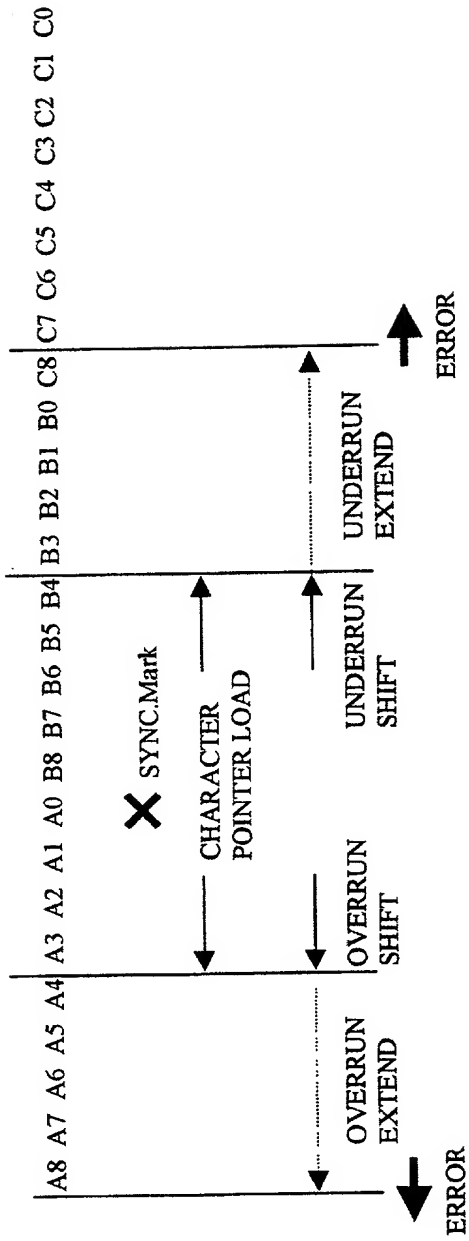


Fig 46

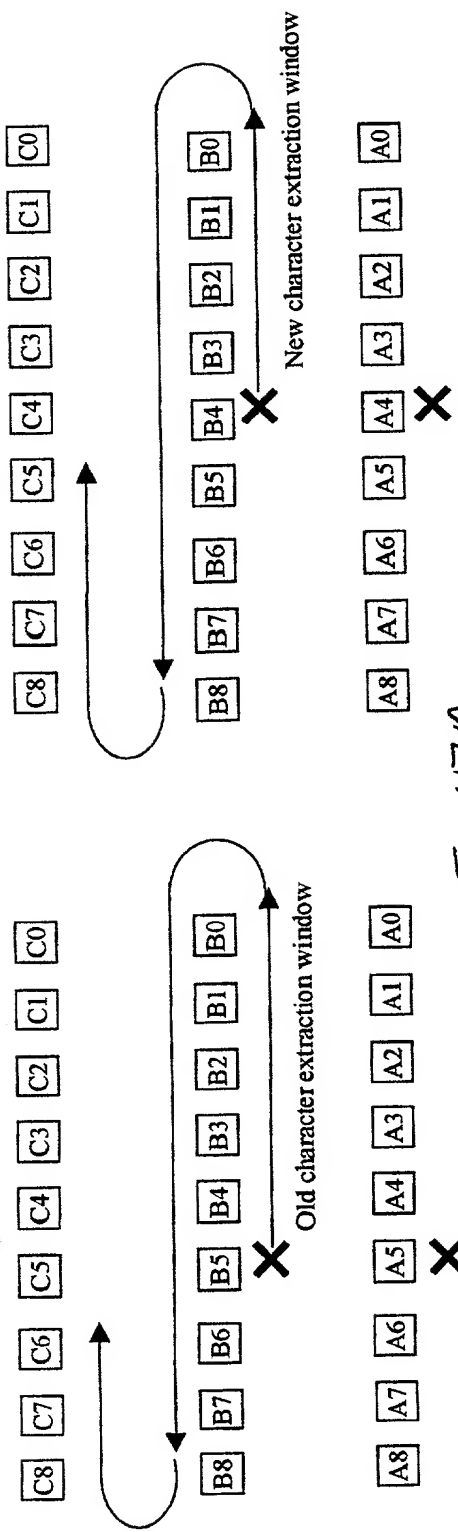


Fig 47A

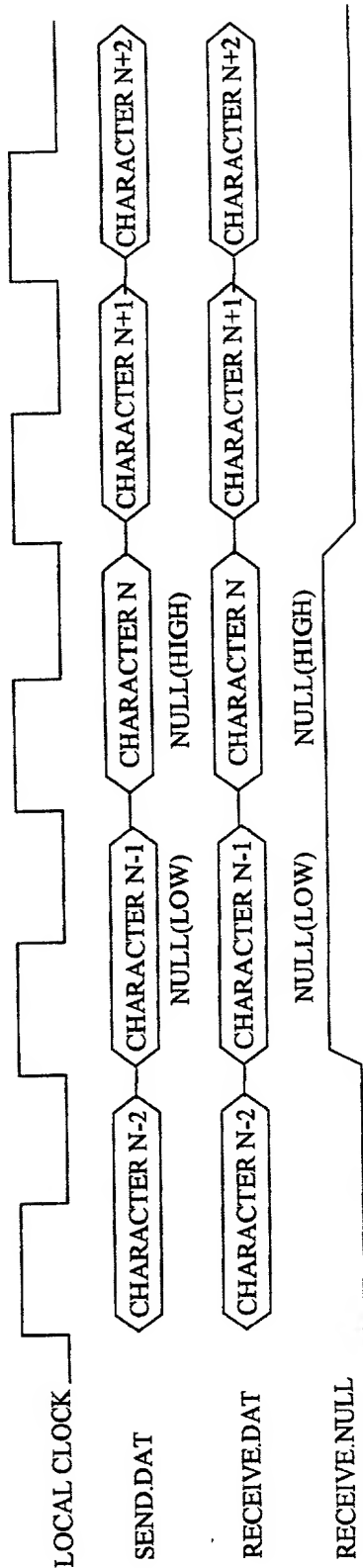


Fig 47B

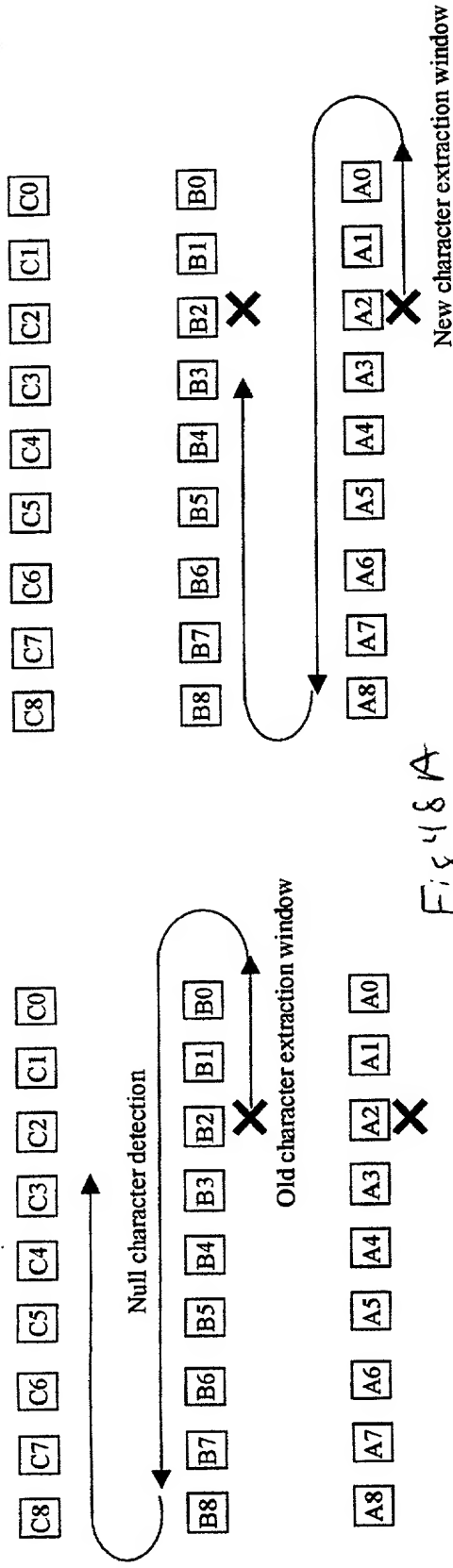


FIG. 48A

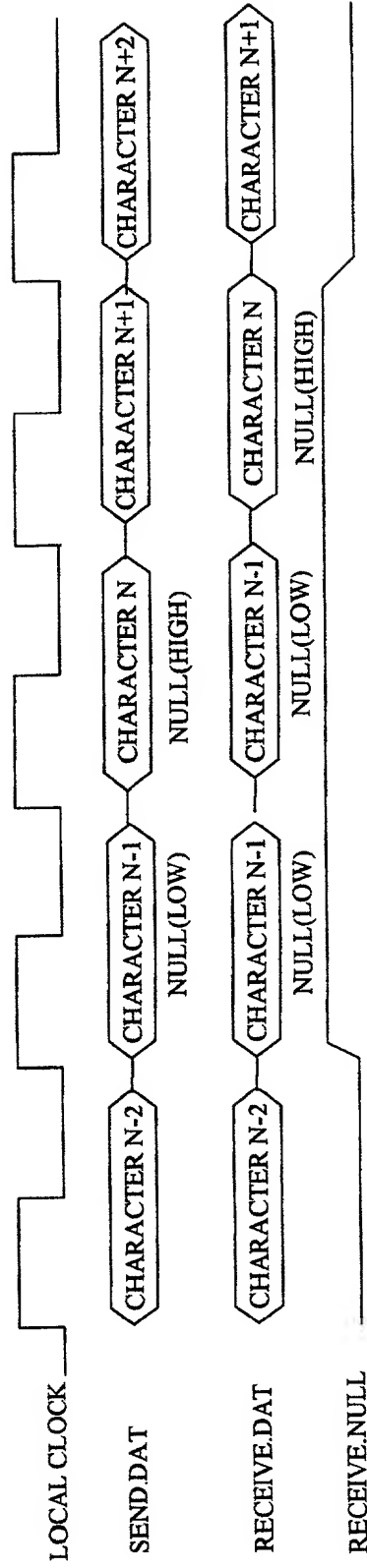


FIG. 48B

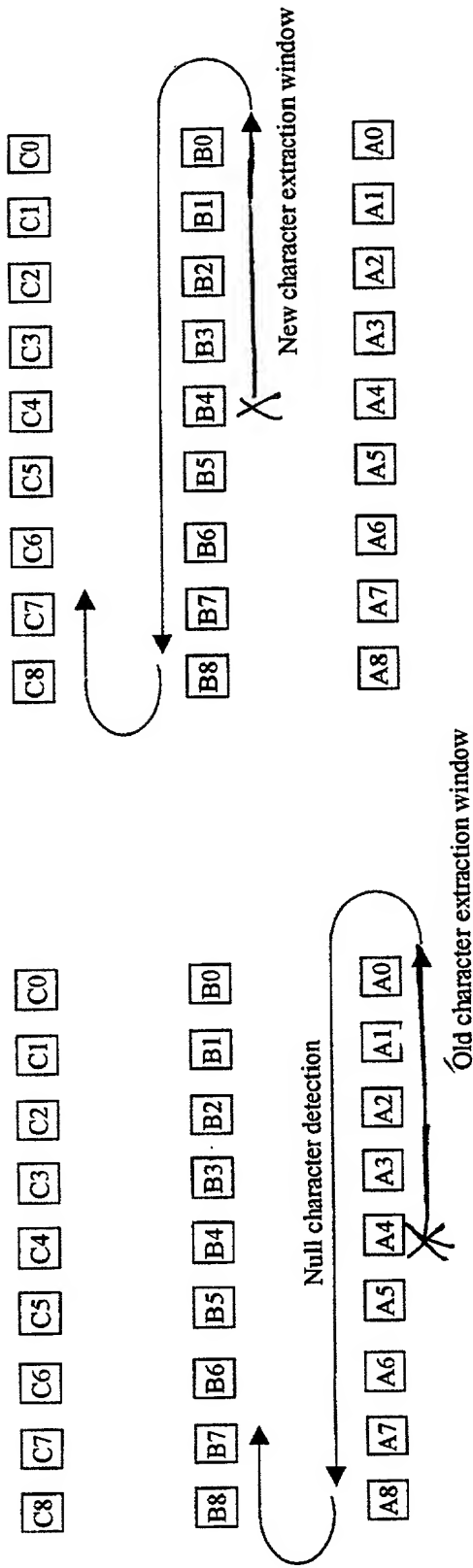


Fig. 49A

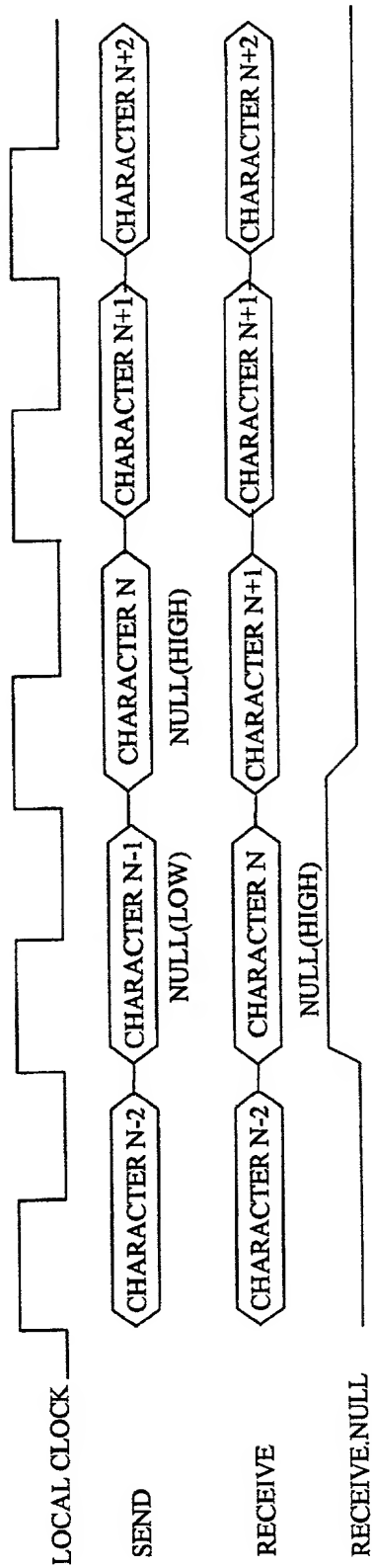


Fig 49B